INTRODUCTION

Colleen is the code name for a video game-home computer product that contains a modified 6502 microprocessor, 4 I/O chips, operating system rom, and expandable ram, and several MSI chips for address decoding and data bus buffering.

This manual is intended to primarily describe the 4 I/O chips in sufficent detail to allow experienced programmers to create the operating system code and to create assembly language application ROMS, such as video games. All 4 Input-Output chips are controlled by the microprocessor by writing directly into their registers which are decoded to exist in microprocessor memory space just as RAM does. These I/O chips can also be interogated by the microprocessor by reading simmilar registers.

It is realy not necessary for the programmer to know which I/O functions are performed by which of the 4 chips, however it does help in learning these functions.

CHIP NAME	FUNCTION
ANTIC	DMA(direct memory access) control. NMI(non maskable interupt) control. Vertical and Horizontal fine scrolling Light pen position registers Vertical line counter WSYN(wait for horiz. sync)

CTIA	Priority control (display of overlaping objects)
	Color- Lum control(colors and brightness assigined to all objects including DMA objects from ANTIC)
	PLAYER-MISSILE objects (4 players & 4 missiles)
	    Graphics registers
	    Size control
	    Horiz. position control
	Collision detection between all objects
	Switches and triggers(misc. I/O functions)

POKEY	Keyboard scan and control Serial communications port (bidirectional) Pot scan (digitizes position of 8 independent pots) Audio generation(4 channels) Timers IRQ(maskable interupt) control Random number generator
PIA	Controller(Joy stick) jacks read or write Peripheral control and interupt lines IRQ(maskable)interupt control from peripherals

The next few pages will introduce some of the concepts needed to understand the Colleen I/O system.

DMA (Direct Menory Access)

The primary function of the Antic chip is to fetch data from memory (independent of the microprocessor) for display on the TV screen. It does this with a technique called"direct memory access" or DMA. It requests the use of the memory address and data bus by sending a signal called HALT to the microprocessor, causing the processor to become "TRI-STATE" (open circuit) all durring the next computer cycle. The ANTIC chip then takes over the address bus and reads any data it wishes from memory. Another name for this type of DMA is "cycle stealing.

Once initiated, this DMA is completly and automatically controled by the Antic chip without need for further microprocessor intervention. The DMA control circuit on the Antic chip resembles a small dumb microprocessor. By halting the main microprocessor it can fetch it's own instructions from memory(the display list) addressed by its program counter (display list pointer). Each instruction defines the type (alpha character or memory map),and the resolution(size of bits on the screen),and the location of data in memory,to be displayed on the next group of lines.

In order to begin this DMA the main microprocessor must store a display list of instructions in memory, store data to be displayed in memory, tell the Antic where the display list is(initalize the display list pointer) and enable the DMA control flags on the Antic(DMACTL register).

In addition to the type of DMA described above,that is used to generate Alpha Numeric characters and memory map (playfield) displays, the Antic chip simultaniously controls another DMA channel. This type of DMA addresses PLAYER-MISSILE graphics data stored in memory and passes the graphics data on to the CTIA chip graphics registers. This type of DMA (if enabled) occurs automatically interspersed with the playfield DMA described previously. This PLAYER-MISSILE DMA has no display list or instructions, and is therefore much simplier than the PLAYFIELD DMA.

In order to begin PLAYER-MISSILE DMA the main microprocessor simply tells the Antic chip where the data is located in memory (loads the player-missile base register PMBASE) and enables the proper DMA control flags on the Antic chip (DMACTL reg.) and on the CTIA chip (GRACTL reg.).

In addition to the two types of DMA described above,the Antic chip also generates DMA addresses for the refresh of the dynamic memory RAMS used in this system. This is also completly automatic and need be considered by the programmer only if he is concerned with real time programming where an exact count of the computer cycles remaining(after the 3 types of DMA have taken their cycles) is important.

The data fetched by the Antic with PLAYFIELD DMA (Alpha characters or memory map) is stored in a shift register and converted into real time serial output for transmission to the CTIA chip where it is assigined a color-luminance,and compared against other displayed objects for collision detection and priority assignment.

The data addressed by Antic PLAYER-MISSILE DMA(players and missiles) is routed directly to shift registers on the CTIA chip where it is converted into real time serial data representing individual players and missiles,which are assigined color-lum values and compared against each other and Playfield for collision detection and priority assignment.

OBJECTS

There are basically two types of objects produced by the I/O chips for display on the TV screen ; graphics objects and playfield objects. Area on the screen where there are no objects is called Background. Background is not the same as blank or black. It is simply the area where objects are not.

Graphics objects are further divided into Players and Missiles. They are limited in width to 8 bits for each player and 2 bits for each missile. Their vertical height is unlimited. Their horizontal position on the screen is determined by a horizontal position register for each object. Player-Missile data can be fetched from memory by the microprocessor or by the Antic chip (using Player-Missile DMA). This data is then stored by the microprocessor(or automatically by DMA) in registers on the CTIA chip where it is held and outputed to the TV screen whenever the horizontal sync counter equals one of the horizontal position registers. Players and missiles will appear as vertical bars unless their data registers are changed by the microprocessor(or by the data in memory if in Player Missile DMA) durring the actual screen display time.

Playfield objects are further divided into Memory map and Characters. Unlike Player-Missile objects that can be moved by simply changing their horiz.position register,Playfield objects have a location on the screen that is determined by their location in memory, and by parameters stored by the microprocessor in the DMA display list in memory. Memory Map playfield data is fetched from memory automatically by the Antic chip where it is placed in a shift register and converted to serial output for the TV display. Character playfield data,in contrast, requires two fetches from memory by the Antic chip. First the Antic fetches the names of the characters from memory and places them in a shift register. These character names are then used to address the actual data which is fetched from memory and converted to serial output for the TV display. All playfield serial output data passes through the CTIA chip before being sent to the TV display.There it is assigined Color-luminance and Priority and tested for Collisions with Graphics objects

COLOR LUM

A color luminance register is used on the CTIA chip for each Player-Missile and Playfield type. Each Color-lum register is loaded by the microprocessor with a code representing the desired color and luminance of it's corresponding Player-Missile or Playfield type. As the serial data passes through the CTIA chip it is "impressed" with the color and luminance values contained in these registers, before being sent to the TV display.

PRIORITY

When moving objects such as players and missiles , overlap on the TV screen(with each other or with Playfield)a decision must be made as to which object shows in front of the other. Objects which appear to pass in front of others are said to have Priority over the ones they pass in front of. Priority is assigined to all objects by the CTIA chip before the serial data from each object is combined with the other objects and sent to the TV screen.

The priority of objects can be controlled by the microprocessor by writing into the control register PRIOR. The functions of the bits in this register are given in the table on page B4.

COLLISIONS

Overlaping objects are considered to have collided. This is detected by a real time occurance of simultanious serial data from more than one object generator. Hardware register bits are used to store 60 of the possible 72 collisions. These collision bits can be read by the Microprocessor as described on pg.11 and B6.

INTERUPTS

Interupts are described extensivly on pg.20. Below is a brief list to itemize the types of interupts provided.

- Instruction interupt.(requested by any display instruction)
- Vertical Blank int.(req.by beginning of vertical blank)
- Reset button int.(req. by pushing reset button on panel)
- Break key int.(req.by pushing break key)
- Other key int.(req.by pushing any key)
- Serial input int. (req.by serial port input)
- Serial output int.(req. by serial port output)
- Transmission finished int.(req.by serial port output)
- Timer interupts (3 each, req.by audio timers)
- Peripheral interupts(2 each, req.by serial port devices)

Almost all of these interupt sources can be masked on command of the microprocessor and have status bits which can be interogated and reset by the microprocessor. Even the interupts defined as "non maskable"(NMI)on the microprocessor have mask bits on the I/O chips which can be set by the microprocessor.

WSYN

In addition to a Vertical Blank Interupt, which allows the microprocessor to synchronize to the vertical TV display, this system also provides a Wait for Horizontal Sync (WSYN) command that allows the Microprocessor to synchronize itself to the TV horizontal line rate. This sync takes effect when the processor writes to an I/O location called WSYN, whenever it desires horizontal synchronization. Writing to this address sets a latch which pulls to zero a pin on the microprocessor called READY. When READY goes to zero the microprocessor stops and waits. The latch is automatically reset(returning READY true) at the beginning of the next horizontal blank interval,releasing the microprocessor to resume program exicution.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
H SCROLL		X		X		X		X		X		X		X		X	Horizontal Scrolling
V SCROLL			X	X			X	X			X	X			X	X	Vertical Scrolling
LD MEM SCAN					X	X	X	X					X	X	X	X	Load memory scan (3 byte)
INST INTERUPT									X	X	X	X	X	X	X	X	Display instruction interupt
BLK 1	00								80								Blank 1 line
" 2	10								90								Blank 2 lines
" 3-7	↓								↓								Blank 3 thru 7 lines
" 8	70								F0								Blank 8 lines
JMP	01								81								Jump (3 byte instruction)
JVB	41								C1								Jump & wait for vert, Blank (ALSO 3 BYTE)
CHR(40,2,8)	02	12	22	32	42	52	62	72	82	92	A2	B2	C2	D2	E2	F2	
" (40,2,10)	03	13	23	33	43	53	63	73	83	93	A3	B3	C3	D3	E3	F3	
" (40,4,8)	04	14	24	34	44	54	64	74	84	94	A4	B4	C4	D4	E4	F4	
" (40,4,16)	05	15	25	35	45	55	65	75	85	95	A5	B5	C5	D5	E5	F5	CHARACTER MODE INSTRUCTIONS
" (20,5,8)	06	16	26	36	46	56	66	76	86	96	A6	B6	C6	D6	E6	F6	
" (20,5,16)	07	17	27	37	47	57	67	77	87	97	A7	B7	C7	D7	E7	F7	
MAP(40,4,8)	08	18	28	38	48	58	68	78	88	98	A8	B8	C8	D8	E8	F8	
" (80,2,4)	09	19	29	39	49	59	69	79	89	99	A9	B9	C9	D9	E9	F9	
" (80,4,4)	0A	1A	2A	3A	4A	5A	6A	7A	8A	9A	AA	BA	CA	DA	EA	FA	
" (160,2,2)	0B	1B	2B	3B	4B	5B	6B	7B	8B	9B	AB	BB	CB	DB	EB	FB	MEMORY MAP MODE INSTRUCTIONS
" (160,2,1)	0C	1C	2C	3C	4C	5C	6C	7C	8C	9C	AC	BC	CC	DC	EC	FC	
" (160,4,2)	0D	1D	2D	3D	4D	5D	6D	7D	8D	9D	AD	BD	CD	DD	ED	FD	
" (160,4,1)	0E	1E	2E	3E	4E	5E	6E	7E	8E	9E	AE	BE	CE	DE	EE	FE	
" (320,2,1)	0F	1F	2F	3F	4F	5F	6F	7F	8F	9F	AF	BF	CF	DF	EF	FF	

Number of TV lines per cell
Number of Colors (Background +Playfield types)
Number of Horizontal cells (Std. width screen)

DISPLAY INSTRUCTION OP-CODES

VERTICAL AND HORIZONTAL FINE SCROLLING

Playfield objects are difficult to move smoothly. Memory map playfield can be moved by rewriting sections of memory,however this is extremely time consuming if large sections of the screen must be moved smoothly. Character playfield objects can be moved easily in a jerkey fasion by changing the memory scan counter, however this results in a large position jump from one character position to another,not a smooth motion. For this reason hardware registers and counters are provided to allow smooth horizontal or vertical motion, up to one character width horizontally and up to one character height vertically. After this much smooth motion has been done by increasing the value in these registers,memory is rewritten or the memory scan counter is modified and smooth motion is resumed for another character distance. The details of the use of these registers is given on pg.12 and pg.A4

LIGHT PEN

A "light pen" input is provided which is connected to the Antic chip. This light pen signal captures the value of the vertical line counter and the horizontal sync counter in two registers, PENV and PENH , whenever the signal goes from true to false because of light falling on the light pen. The microprocessor can then read these two registers to determine the pen vertical and horizontal position.

VERTICAL LINE COUNT

The microprocessor can also read a location that contains the present TV line number being displayed. This allows the microprocessor to modify the display depending on the present vertical location of the TV spot creating the display.

OBJECT GENERATION

OBJECTS CAN BE GENERATED EITHER AS PLAYFIELD OR AS PLAYER-MISSILE GRAPHICS. (SEE PG 2) THESE ARE TWO DISTINCT, ALMOST INDEPENDENT, OBJECT GENERATING CIRCUITS.

PLAYER-MISSILE GRAPHICS GENERATION

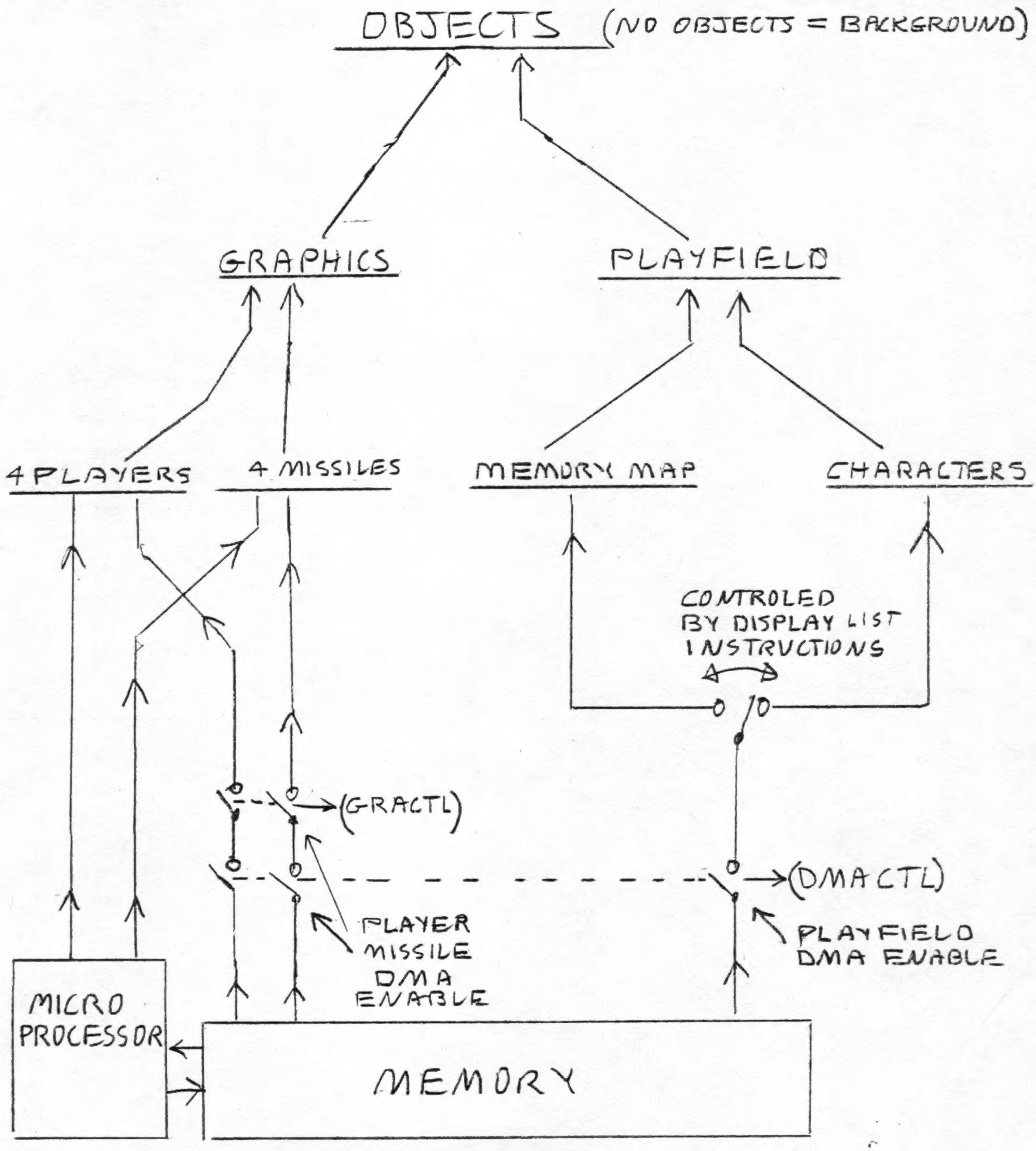
THERE ARE 8 GRAPHIC OBJECTS, 4 PLAYERS AND 4 MISSILES. THE 4 MISSILES MAY BE GROUPED TOGETHER AND USED AS A 5TH PLAYER. THESE OBJECTS ARE POSITIONED HORIZONTALLY BY 8 HORZ. POSITION REGISTERS. (HPOS(X)). THESE REGISTERS MAY BE RELOADED AT ANY TIME BY THE PROCESSOR, ALLOWING AN OBJECT TO BE REPLICATED MANY TIMES ACROSS A HORIZONTAL TV LINE.

THE SHAPE OF A PLAYER-MISSILE IS DETERMINED BY THE DATA IN ITS GRAPHICS REGISTER (GRAF(X)). PLAYERS HAVE INDEPENDENT 8 BIT GRAPHIC REGISTERS. THE FOUR MISSILES HAVE 2 BIT REGISTERS (LOCATED WITHIN ONE ADDRESS). THESE REGISTERS MAY ALSO BE RELOADED AT ANY TIME BY THE PROCESSOR, ALTHOUGH THEY ARE USEUALY CHANGED DURING HORIZONTAL BLANK TIME. THE DATA IN EACH GRAPHICS REGISTER IS PLACED ON THE DISPLAY WHENEVER THE HORIZONTAL SYNC COUNTER EQUALS THE CORRESPONDING HORIZONTAL POSITION REGISTER. THE SAME DATA WILL BE DISPLAYED EVERY LINE UNLESS THE GRAPHIC REGISTERS ARE RELOADED WITH NEW DATA.

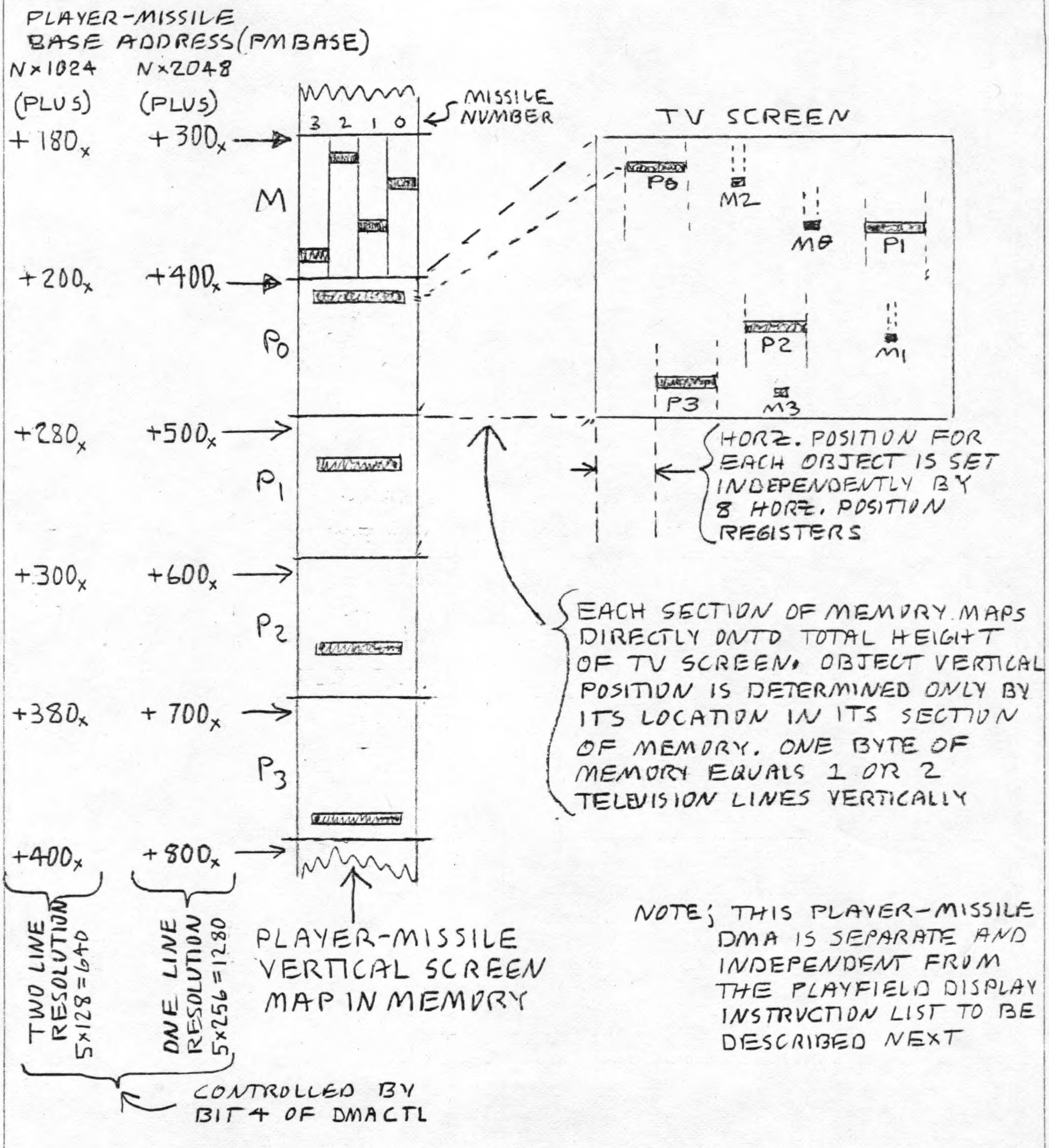
THE PLAYER-MISSILE GRAPHIC REGISTERS MAY BE RELOADED BY THE MICROPROCESSOR (GRAF(X)), OR AUTOMATICALLY DIRECTLY FROM MEMORY WITH DIRECT MEMORY ACCESS (DMA). THE PROGRAMER MUST PLACE THE OBJECT GRAPHICS IN MEMORY, (SEE PG 3), WRITE THE PLAYER-MISSILE BASE ADDRESS (PMBASE), AND ENABLE PLAYER-MISSILE DMA (DMACTL, GRACTL). THE TRANSFER OF OBJECT GRAPHICS FROM MEMORY TO DISPLAY IS THEN FULLY AUTOMATIC.

PLAYFIELD GENERATION

PLAYFIELD IS ALLWAYS GENERATED BY DMA. THERE ARE 4 TYPES OF PLAYFIELD, EACH IDENTIFIED BY ITS OWN COLOR-LUM REGISTER AND COLLISION DETECTION. PLAYFIELD IS GENERATED BY TWO DIFFERENT DMA TECHNIQUES; MEMORY MAP AND CHARACTER. BOTH METHODS PROVIDE AUTOMATIC DMA DISPLAY, CONTROLED BY A DISPLAY LIST OF INSTRUCTIONS IN MEMORY, INDEPENDENT OF THE PLAYER-MISSILE GENERATION



OBJECT DISPLAY SOURCES



NOTE; THIS PLAYER-MISSILE DMA IS SEPARATE AND INDEPENDENT FROM THE PLAYFIELD DISPLAY INSTRUCTION LIST TO BE DESCRIBED NEXT

PLAYER-MISSILE DMA

PLAYFIELD DMA

DISPLAY LIST

THE DISPLAY LIST IS A SEQUENCE OF DISPLAY INSTRUCTIONS STORED IN MEMORY. THESE INSTRUCTIONS ARE EITHER ONE BYTE, OR 3 BYTES LONG. THE DISPLAY LIST CAN BE CONSIDERED A DISPLAY PROGRAM, AND THE DISPLAY LIST COUNTER THAT FETCHES THESE INSTRUCTIONS CAN BE THOUGHT OF AS A DISPLAY PROGRAM COUNTER. (10 BIT COUNTER PLUS 6 BIT BASE REG.)

THE DISPLAY LIST COUNTER CAN BE INITALIZED AT ANY TIME BY WRITING TO DLISTH AND DLISTL. ONCE INITALIZED THIS COUNTER VALUE IS USED TO ADDRESS THE DISPLAY LIST, FETCH THE INSTRUCTION, DISPLAY 1 TO 16 LINES OF DATA ON THE TV SCREEN, INCREMENT THE DISPLAY LIST COUNTER, FETCH THE NEXT DISPLAY INSTRUCTION, AND SO ON AUTOMATICALLY WITHOUT MICROPROCESSOR CONTROL. (SEE PG. A1 FOR DLIST BITS)

EACH INSTRUCTION DEFINES THE TYPE (ALPHA CHARACTER OR MEMORY MAP) AND THE RESOLUTION (SIZE OF BITS ON SCREEN) AND THE LOCATION OF DATA IN MEMORY TO BE DISPLAYED, FOR A GROUP (1 TO 16) OF LINES. EACH GROUP OF LINES IS CALLED A DISPLAY BLOCK.

DISPLAY INSTRUCTION FORMAT

EACH INSTRUCTION CONSISTS OF EITHER AN OPCODE ONLY, OR OF AN OPCODE FOLLOWED BY 2 BYTES OF OPERAND.

OPCODE	} SINGLE BYTE DISPLAY INSTRUCTION

OPCODE	}
OPERAND	} TRIPLE BYTE DISPLAY INSTRUCTION
OPERAND	}

THE OPCODE IS ALLWAYS FETCHED FIRST AND PLACED IN THE INSTRUCTION REGISTER. THIS OPCODE DEFINES THE TYPE OF INSTRUCTION (ONE OR THREE BYTE) AND WILL CAUSE TWO MORE BYTES TO BE FETCHED IF NEEDED. IF FETCHED, THESE NEXT 2 BYTES WILL BE PLACED IN THE MEMORY SCAN COUNTER, OR IN THE DISPLAY LIST COUNTER (IF INSTRUCTION IS A JUMP).

DISPLAY INSTRUCTION REGISTER

THIS REGISTER IS NOT DIRECTLY ACCESSABLE BY THE PROGRAMER. IT IS LOADED WITH THE OPCODE OF EACH INSTRUCTION.

D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	0	0	0	0	BLANK 1 LINE
X	0	0	1	0	0	0	0	BLANK 2 LINES
								ETC.
X	1	1	1	0	0	0	0	BLANK 8 LINES
0	X	X	X	X	X	X	X	NO INTERUPT
1	X	X	X	X	X	X	X	INTERUPT (BIT 7 OF NMI STATUS)
X	0	X	X	0	0	0	1	JUMP
X	1	X	X	0	0	0	1	JUMP AND WAIT (NO DISPLAY) UNTILL END OF NEXT VERTICAL BLANK TIME. (JUMPS ARE 3 BYTES AND THEY RELOAD DISPLAY LIST COUNTER)

BLANK 1 LINE – BLANK 8 LINES: ACTUALLY BACK GROUND COLOR-LUM NOT BLACK.

D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	NO INTERUPT
1	X	X	X	X	X	X		INTERUPT (BIT 7 OF NMI STATUS)
	0	X	X	X	X	X	X	ONE BYTE INST.
	1	X	X	X	X	X	X	3 BYTE INST. (RELOAD MEM. SCAN COUNTER)
		0	X	X	X	X	X	NO VERTICAL SCROLL
		1	X	X	X	X	X	VERTICAL SCROLL
			0	X	X	X	X	NO HORIZONTAL SCROLL
			1	X	X	X	X	HORIZONTAL SCROLL

D3–D0: DISPLAY MODE OP CODES (JUMP + BLANK EXCLUDED) SEE LIST OF DISPLAY MODES ON PG. 7 10 + 11.

MEMORY SCAN COUNTER

THIS COUNTER IS NOT DIRECTLY ACCESSABLE BY THE PROGRAMER. IT IS LOADED WITH THE VALUE IN THE LAST 2 BYTES OF A 3 BYTE (NON JUMP) INSTRUCTION.

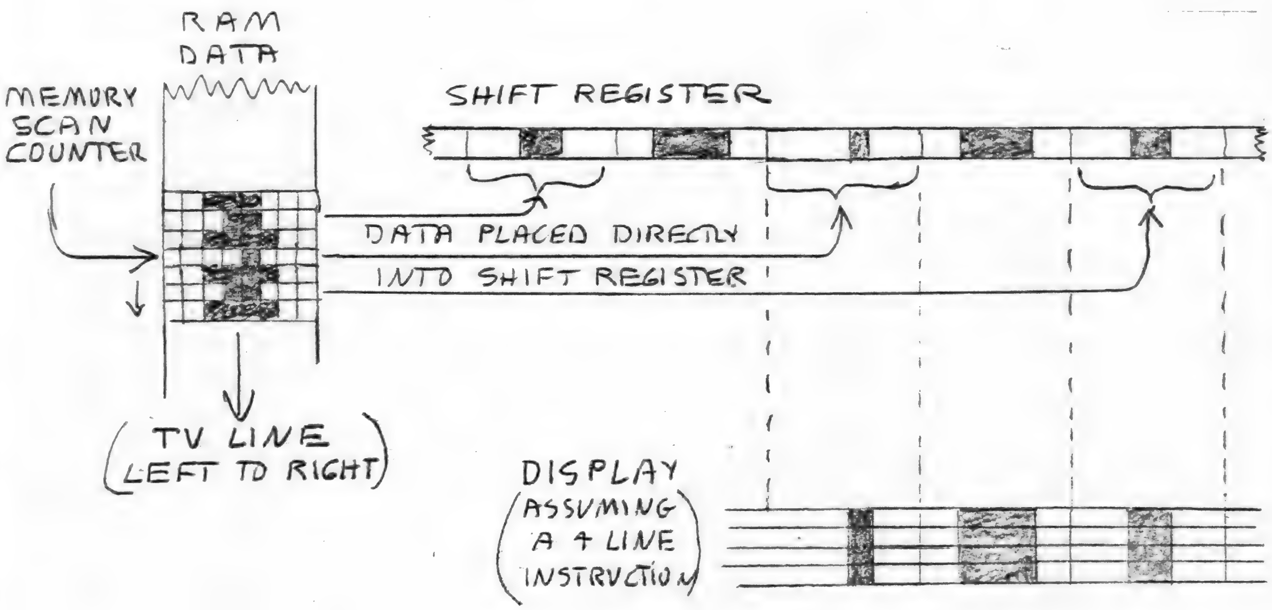
THIS COUNTER POINTS TO THE LOCATION (ADDRESS) IN MEMORY OF DATA TO BE DIRECTLY DISPLAYED (MEMORY MAP DISPLAY) OR TO THE LOCATION OF CHARACTER NAME STRINGS TO BE INDIRECTLY DISPLAYED (CHARACTER DISPLAY).

A SINGLE BYTE INSTRUCTION DOES NOT RELOAD THIS COUNTER. THIS IMPLIES A CONTINUATION IN MEMORY OF DATA TO BE DISPLAYED FROM THAT DISPLAYED BY THE PREVIOUS INSTRUCTION. SINCE THIS COUNTER REALY

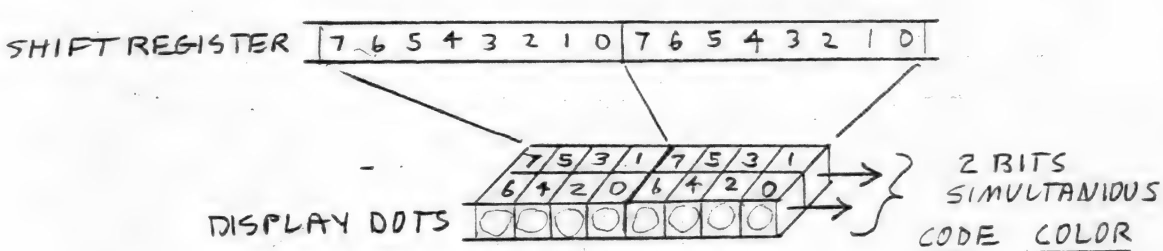
CONSISTS OF 4 BITS OF REGISTER AND 12 BITS OF ACTUAL COUNTER, A CONTINUOUS MEMORY BLOCK CANNOT CROSS 4 K BYTE MEMORY BOUNDARIES, UNLESS THE COUNTER IS REPOSITIONED WITH A 3 BYTE TYPE OF INSTRUCTION. (NON JUMP 3 BYTE INSTRUCTION)

MEMORY MAP DISPLAYS

DISPLAY DATA IS FETCHED DIRECTLY BY THE MEMORY SCAN COUNTER AND PLACED IN A SHIFT REGISTER. THIS SHIFT REGISTER IS USED TO DISPLAY AS MANY LINES AS REQUIRED BY THE DISPLAY INSTRUCTION.



SOME INSTRUCTIONS COMPRESS DATA IN THE SHIFT REGISTER TO GIVE A TWO BIT DEEP DISPLAY. THE TWO BITS OF DEPTH ALLOW EACH DISPLAY DOT TO BE IDENTIFIED AS BACKGROUND (BOTH BITS ZERO) OR AS ONE OF 3 TYPES OF PLAYFIELD.



CODE	COLOR
00	BKGND.
01	PF1
10	PF2
11	PF3

MEMORY MAP DISPLAY INSTRUCTIONS

DATA IN MEMORY (ADDRESSED BY THE MEMORY SCAN COUNTER) IS DISPLAYED DIRECTLY WHEN EXECUTING A MEMORY MAP DISPLAY INSTRUCTION. AS DATA IS BEING DISPLAYED IT IS ALSO STORED IN A SHIFT REGISTER SO THAT IT CAN BE REDISPLAYED FOR AS MANY TV LINES AS REQUIRED BY THE INSTRUCTION.

(INSTRUCTION REGISTER BITS)

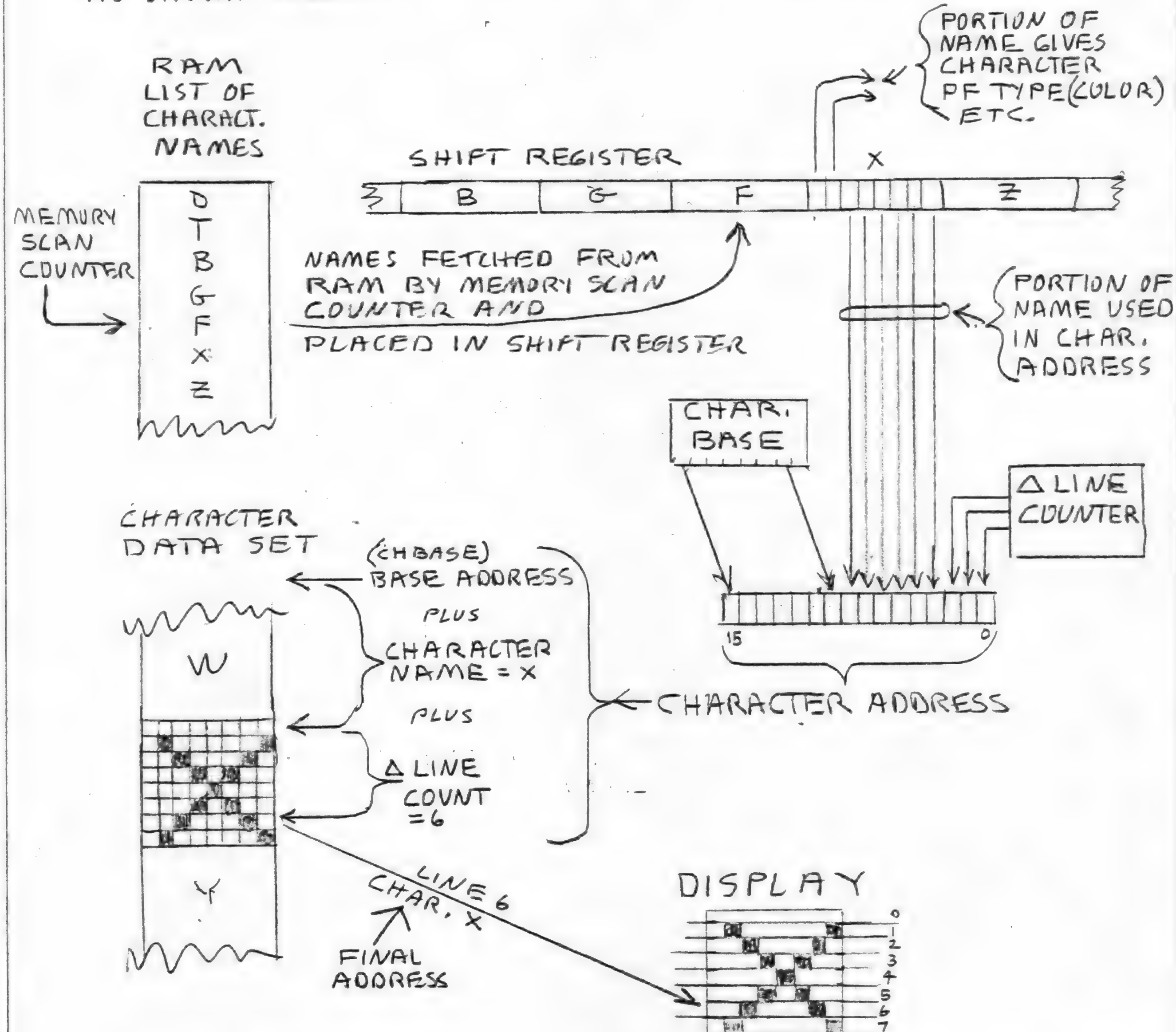
3 2 1 0	OUTPUT DISPLAYED BY EACH BYTE	STD. HORIZ. BITS DISPLD.	COLOR LUM	INST. VERT TV LINES	
1 1 1 1	7/6/5/4/3/2/1/0 — ½ CLOCK → ← — 1 TV LINE	320	PF2 PF1 (LUM ONLY)	1	8
1 1 1 0	7/5/3/1, 6/4/2/0 — 1 CLOCK → ← — 1 TV LINE	160	BK PFθ PF1 PF2	1	
1 1 0 1	7/5/3/1, 6/4/2/0 — 1 CLOCK → ← — 2 TV LINES	160	BK PFθ PF1 PF2	2	7
1 1 0 0	1 CLOCK → ← — 1 TV LINE	160	BK PFθ	1	6
1 0 1 1	1 CLOCK → ← — 2 TV LINES	160	BK PFθ	2	
1 0 1 0	2 CLOCKS → ← — 4 TV LINES	80	BK PFθ PF1 PF2	4	5
1 0 0 1	2 CLOCKS → ← — 4 TV LINES	80	BK PFθ	4	4
1 0 0 0	4 CLOCKS → ← — 8 TV LINES	40	BK PFθ PF1 PF2	8	3

NOTE; ALL MEMORY MAP AND CHARACTER INSTRUCTIONS DISPLAY DATA AS AS ONE OF 4 TYPES OF PLAYFIELD OR BACKGROUND, EACH WITH IT'S OWN SEPARATE COLOR-LUM REGISTER.

(M) = Display mode # (O.S.)

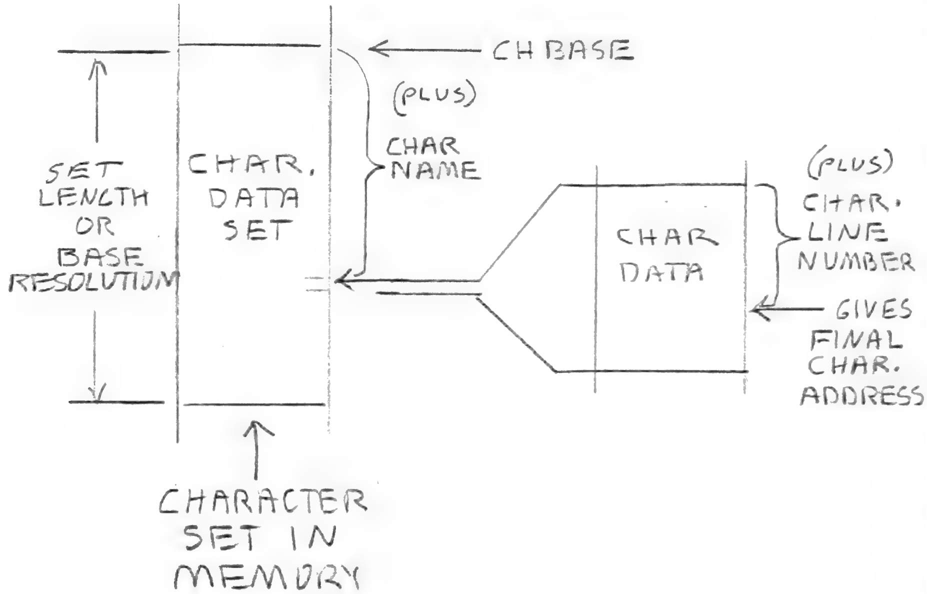
CHARACTER DISPLAYS

CHARACTER NAMES (CODES) ARE FETCHED BY THE MEMORY SCAN COUNTER, AND ARE PLACED IN A SHIFT REGISTER. ON ANY GIVEN LINE OF DISPLAY, THE SHIFT REGISTER ROTATES CHANGING ONLY THE NAME PORTION OF THE CHARACTER ADDRESS. AS SHOWN BELOW.



AFTER A FULL LINE OF CHARACTER DATA HAS BEEN DISPLAYED THE Δ LINE COUNTER INCREMENTS. THE NEXT LINE AGAIN ADDRESSES ALL CHARACTERS BY NAME FOR THAT Δ LINE NUMBER.

ONLY THE MOST SIGNIFICANT 5, OR 6 BITS OF THE CHARACTER BASE REGISTER ARE USED IN THE FINAL ADDRESS, DEPENDING ON THE INSTRUCTION TYPE. CHARACTER SETS THEREFORE COME IN 2 DIFFERENT SIZES; 512, AND 1024 TOTAL BYTES (MAX).



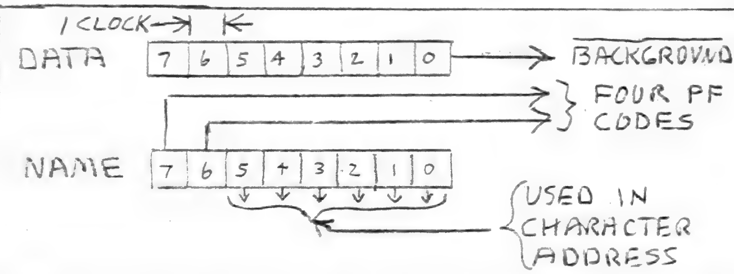
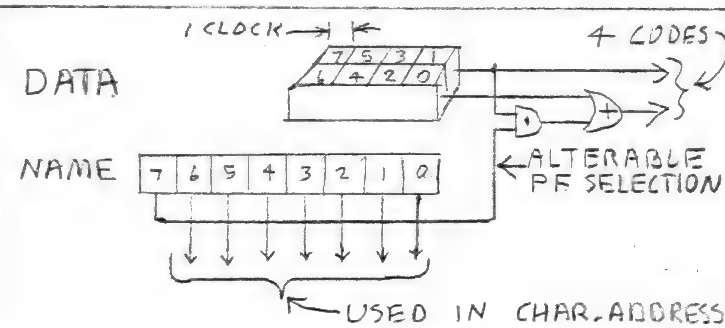
CHAR. INSTRUCT. CODE	CHAR DISPLAY TYPE	SET LENGTH (BASE RESOLUTION)	NUMBER OF CHAR. IN SET	BYTES PER CHAR
011X	20×5	512 BYTES	64	8
010X	40×4	1024 BYTES	128	8
001X	40×2	1024 BYTES	128	8

BASE = N × BLOCK LENGTH

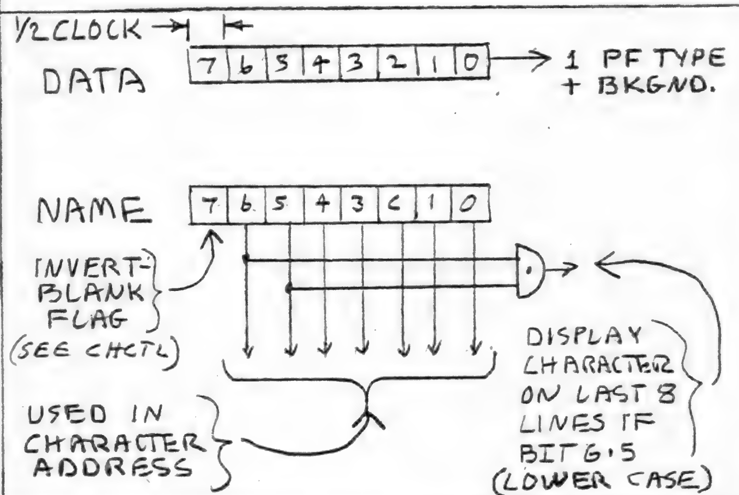
DIFFERENT PORTIONS OF THE CHARACTER NAME ARE USED IN THE FINAL ADDRESS, ALSO DEPENDING ON THE INSTRUCTION TYPE AS SHOWN IN THE FOLLOWING LIST OF CHARACTER INSTRUCTIONS.

CHARACTER DISPLAY INSTRUCTIONS

DATA IN MEMORY (ADDRESSED BY THE MEMORY SCAN COUNTER) IS NOT DISPLAYED DIRECTLY WHEN EXECUTING A CHARACTER DISPLAY INSTRUCTION. THE MEMORY SCAN COUNTER POINTS INSTEAD TO A LIST OF CHARACTER NAMES. THIS LIST OF NAMES MIGHT FOR EXAMPLE CONTAIN THE ASCI CODE NAMES FOR ALPHA-NUMERIC CHARACTERS TO BE DISPLAYED. THIS NAME LIST IS FETCHED BY THE MEMORY SCAN COUNTER AND PLACED IN A SHIFT REGISTER. THESE CHARACTER NAMES ARE THEN COMBINED WITH THE TV LINE COUNT, AND THE CHARACTER BASE ADDRESS, TO CREATE THE CHARACTER ADDRESS THAT ACTUALLY FETCHES CHARACTER DATA TO BE DISPLAYED. (SEE "CHBASE" PG.___)

IR BITS 3 2 1 0	OUTPUT DISPLAYED BY EACH BYTE (ALL CHARACTERS ARE 8 BYTES HIGH)	STD HORZ CHAR. DISPLD.	COLOR LUM	INST. VERT. TV LINES
0111 (20×5)		20	BK PF0 PF1 PF2 PF3 = 5	16
0110	SAME AS ABOVE EXCEPT EACH DATA BYTE SHOWN FOR 1 LINE INSTEAD OF 2	20	SAME↑	8
0101 (40×4)		40	BK PF0 PF1 PF2 = 4	16
0100	SAME AS ABOVE EXCEPT EACH DATA BYTE SHOWN FOR 1 LINE INSTEAD OF 2	40	SAME↑	8

CHARACTER DISPLAY INSTRUCTIONS

INSTR. REG. BITS 3 2 1 0	OUTPUT DISPLAYED BY EACH BYTE (CHARACTERS ARE ALL 8 BYTES HIGH)	STD HORZ. CHARS. DISPLD.	COLOR LUM	INST. VERT TV LINES
0011 (40 × 2)		40	BK PF0 = 2	10
0010	SAME AS ABOVE EXCEPT ONLY 8 LINES TOTAL FOR EACH INSTRUCTION	40	SAME↑	8

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VERTICAL SCROLLING, DETAILS OF OPERATION

FOR VERTICAL SCROLLING OF A ZONE OF DISPLAY ON THE SCREEN, THE DISPLAY BLOCKS AT THE UPPER AND LOWER BOUNDRIES OF THAT ZONE MUST HAVE A VARIABLE VERTICAL SIZE. IN PARTICULAR, THE FIRST DISPLAY BLOCK WITHIN THAT ZONE MUST BE SHORTENED FROM THE TOP, AND THE LAST DISPLAY BLOCK MUST BE SHORTENED FROM THE BOTTOM.

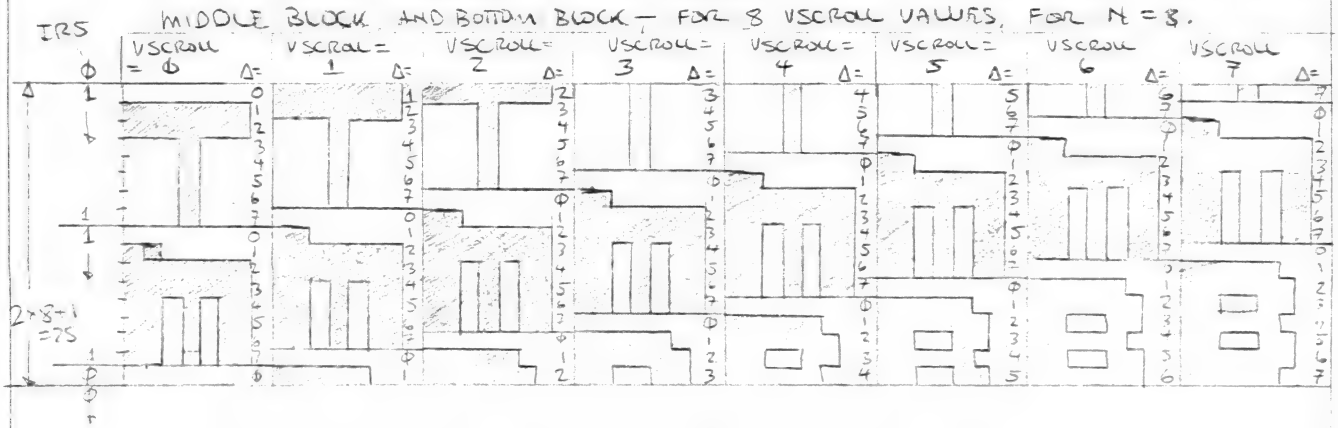
THE VERTICAL DIMENSION OF EACH DISPLAY BLOCK IS CONTROLLED BY A 4 BIT COUNTER WITHIN THE ANTIC, CALLED THE 'DELTA COUNTER' (DCTR). WITHOUT VERTICAL SCROLLING, IT STARTS AT Ø ON THE FIRST LINE, AND COUNTS UP TO A STANDARD VALUE, DETERMINED BY THE CURRENT DISPLAY INSTRUCTION. (EX: FOR UPPER & LOWER CASE TEXT DISPLAY, THE END VALUE IS 9; FOR 5 COLOR CHARACTER DISPLAYS, IT IS 7 OR 15)

BIT 5 OF THE INSTRUCTION CONTROLS VERTICAL SCROLLING; IN PARTICULAR, CHANGES IN BIT 5 BETWEEN CONSECUTIVE INSTRUCTIONS IN THE DISPLAY LIST. IF BIT 5 GOES FROM Ø TO 1 BETWEEN TWO DISPLAY BLOCKS, THE SECOND BLOCK WILL START WITH THE DELTA COUNTER LOADED WITH THE 4 BIT VALUE IN THE VSCROLL REGISTER, INSTEAD OF Ø, SHORTENING IT FROM THE TOP.

IF BIT 5 OF THE INSTRUCTION GOES FROM 1 TO Ø BETWEEN TWO CONSECUTIVE DISPLAY BLOCKS, THE SECOND BLOCK WILL START WITH DELTA = Ø, AS USUAL, BUT WILL COUNT UP UNTIL DELTA = VSCROLL INSTEAD OF THE STANDARD VALUE; THIS SHORTENS THAT DISPLAY BLOCK FROM THE BOTTOM.

IF BIT 5 OF THE INSTRUCTION DOES NOT CHANGE BETWEEN CONSECUTIVE DISPLAY BLOCKS, VERTICAL SCROLLING DOES NOT OCCUR.

TO DEFINE A VERTICALLY SCROLLED ZONE, THE MOST DIRECT METHOD IS TO SET BIT 5 = 1 IN THE FIRST DISPLAY INSTRUCTION FOR THAT ZONE, AND IN ALL CONSECUTIVE BLOCKS BUT THE LAST ONE. IF THE VSCROLL REGISTER IS NOT REWRITTEN ON THE FLY, THIS RESULTS IN A TOTAL SCROLLED ZONE THAT HAS A CONSTANT NUMBER OF LINES (PROVIDED THAT THE VSCROLL VALUE DOES NOT EXCEED THE STANDARD INDIVIDUAL BLOCK SIZE). IF N IS THE STANDARD BLOCK SIZE, THE TOP BLOCK WILL BE N - VSCROLL LINES (N > VSCROLL), AND THE LAST BLOCK WILL BE VSCROLL + 1 LINES: (N - VSCROLL) + VSCROLL + 1 = N + 1. SHOWN BELOW IS AN EXAMPLE OF A SCROLLED ZONE, - TOP BLOCK, MIDDLE BLOCK AND BOTTOM BLOCK - FOR 8 VSCROLL VALUES, FOR N = 8.



AUDIO

THERE ARE 4 SEMI-INDEPENDENT AUDIO CHANNELS, EACH WITH ITS OWN FREQUENCY, NOISE, AND VOLUME CONTROL. EACH HAS AN 8 BIT "DIVIDE BY N" FREQUENCY DIVIDER, CONTROLED BY AN 8 BIT REGISTER (AUDFX). (SEE AUDIO-SERIAL PORT BLOCK DIAGRAM) EACH CHANNEL ALSO HAS AN 8 BIT CONTROL REGISTER (AUDCX) WHICH SELECTS THE NOISE (POLY COUNTER) CONTENT, AND THE VOLUME.

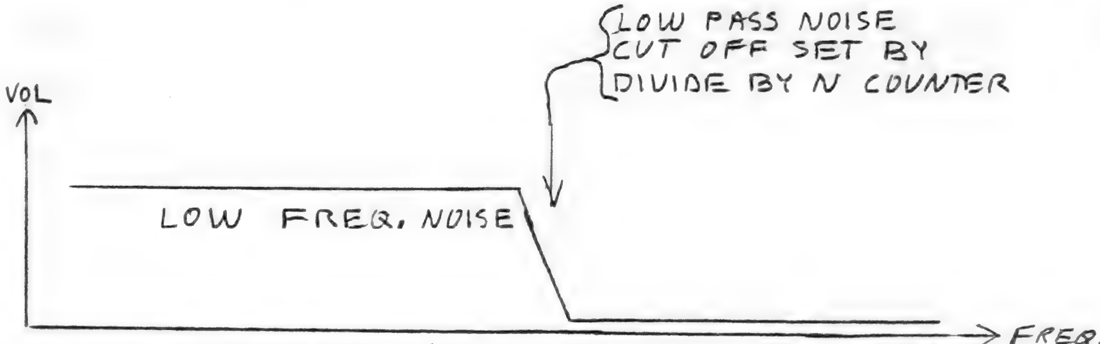
FREQUENCY DIVIDERS

ALL 4 FREQ. DIVIDERS CAN BE CLOCKED SIMULTANIOUSLY FROM 64 KHZ OR 15 KHZ. (AUDCTL BIT 0). FREQ. DIVIDERS 1 AND 3 CAN ALTERNATELY BE CLOCKED FROM 1.79 MHZ (AUDCTL BIT 6,5). DIVIDERS 2 AND 4 CAN ALTERNATELY BE CLOCKED WITH THE OUTPUT OF DIVIDERS 1 AND 3 (AUDCTL BITS 4,3) THIS ALLOWS THE FOLLOWING OPTIONS; 4 CHANNELS OF 8 BITS RESOLUTION, 2 CHANNELS OF 16 BIT RESOLUTION, OR 1 CHANNEL OF 16 BIT AND 2 CHANNELS OF 8 BIT.

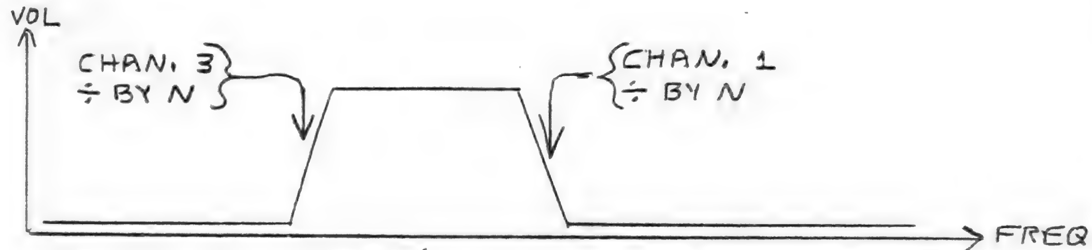
POLY NOISE COUNTERS

THERE ARE 3 POLYNOMIAL COUNTERS (17 BIT, 5 BIT AND 4 BIT) USED TO GENERATE RANDOM NOISE. THE 17 BIT POLY COUNTER CAN BE REDUCED TO 9 BITS (AUDCTL BIT 7). THESE COUNTERS ARE ALL CLOCKED BY 1.79 MHZ. THEIR OUTPUTS HOWEVER CAN BE SAMPLED INDEPENDENTY BY THE FOUR AUDIO CHANNELS AT A RATE DETERMINED BY EACH CHANNEL'S FREQUENCY DIVIDER. THUS EACH CHANNEL APPEARS TO CONTAIN SEPARATE POLY COUNTERS (3 TYPES) CLOCKED AT ITS OWN FREQUENCY. THIS POLY COUNTER NOISE SAMPLING IS CONTROLLED BY BITS 5, 6, AND 7 OF EACH AUDCX REGISTER. BECAUSE THE POLY, COUNTERS ARE SAMPLED BY THE "DIVIDE BY N" FREQUENCY DIVIDER, THE OUTPUT OBVIOUSLY CANNOT CHANGE FASTER THAN THE SAMPLING RATE. IN THESE MODES (POLY NOISE OUTPUTED) THE DIVIDERS ARE THEREFORE ACTING AS "LOW PASS" FILTER CLOCKS, ALLOWING ONLY THE LOW FREQUENCY NOISE TO PASS.

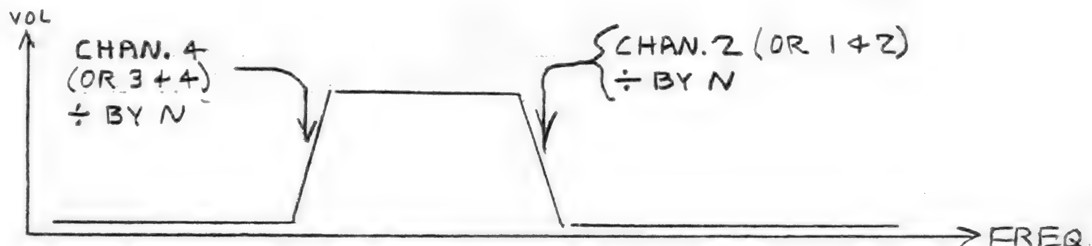
THE OUTPUT OF THE NOISE CONTROL CIRCUIT DESCRIBED ABOVE CONSISTS OF PURE TONES (SQUARE WAVE TYPE), OR POLYNOMIAL COUNTER NOISE AT A MAXIMUM FREQUENCY SET BY THE "DIVIDE BY N" COUNTER (LOW PASS CLOCK). THIS OUTPUT CAN BE ROUTED THROUGH A HIGH PASS FILTER IF DESIRED. (AUDCTL BITS 1 AND 2).



ANY CHANNEL NOISE OUTPUT (WITHOUT HIGH PASS FILTER)



CHANNEL 1 OUTPUT (WITH HIGH PASS FILTER)



CHANNEL 2 OUTPUT (WITH HIGH PASS FILTER)

AUDIO NOISE FILTERS

HIGH PASS FILTERS

THE HIGH PASS FILTER CONSISTS OF A "D" FLIP FLOP AND AN EXCLUSIVE-OR GATE. THE NOISE CONTROL CIRCUIT OUTPUT IS SAMPLED BY THIS FLIP FLOP AT A RATE SET BY THE "HIGH PASS" CLOCK. THE INPUT AND OUTPUT OF THE FLIP FLOP PASS THROUGH THE EXCLUSIVE-OR GATE. IF THE FLIP FLOP INPUT IS CHANGING MUCH FASTER THAN THE CLOCK RATE, THE SIGNAL WILL PASS EASILY THROUGH THE EX.-OR GATE. HOWEVER IF IT IS LOWER THAN THE CLOCK RATE, THE FLIP FLOP OUTPUT WILL TEND TO FOLLOW THE INPUT AND THE TWO EX.-OR GATE INPUTS WILL MOSTLY BE IDENTICAL (11 OR 00) GIVING VERY LITTLE OUTPUT. THIS GIVES THE EFFECT OF A CRUDE HIGH PASS FILTER, PASSING NOISE WHOSE MINIMUM FREQUENCY IS SET BY THE HIGH PASS CLOCK RATE. ONLY CHANNELS 1 AND 2 HAVE SUCH A HIGH PASS FILTER. THE HIGH PASS CLOCK FOR CHANNEL 1 COMES FROM CHANNEL 3 DIVIDER. THE HIGH PASS CLOCK FOR CHANNEL 2 COMES FROM CHANNEL 4 DIVIDER. THIS FILTER IS INCLUDED ONLY IF BIT 1 OR 2 OF AUDCTL IS TRUE.

VOLUME CONTROL

A VOLUME CONTROL CIRCUIT IS PLACED AT THE OUTPUT OF EACH CHANNEL. THIS IS A CRUDE 4 BIT DIGITAL TO ANALOG CONVERTER THAT ALLOWS SELECTION OF ONE OF 16 POSSIBLE OUTPUT CURRENT LEVELS FOR A LOGIC TRUE AUDIO INPUT. A LOGIC ZERO AUDIO INPUT TO THIS VOLUME CIRCUIT ALLWAYS GIVES AN OPEN CIRCUIT (ZERO CURRENT) OUTPUT. THE VOLUME SELECTION IS CONTROLED BY BITS 0 THRU 3 OF AUDCX. "VOLUME CONTROL ONLY" MODE CAN BE INVOKED BY FORCING THIS CIRCUIT'S AUDIO INPUT TRUE WITH BIT 4 OF AUDCX. IN THIS MODE THE DIVIDERS, NOISE COUNTERS, AND FILTER CIRCUITS ARE ALL DISCONNECTED FROM THE CHANNEL OUTPUT. ONLY THE VOLUME CONTROL BITS (0-3 OF AUDCX) DETERMINE THE CHANNEL OUTPUT CURRENT.

THE AUDIO OUTPUT OF ANY CHANNEL CAN BE COMPLETLY TURNED OFF BY WRITING ZEROS TO THE VOLUME CONTROL BITS OF AUDCX. ALL ONES GIVES MAXIMUM VOLUME.

SERIAL PORT

GENERAL THE SERIAL PORT CONSISTS OF A SERIAL DATA OUTPUT (TRANSMISSION) LINE, A SERIAL DATA INPUT (RECEIVER) LINE, A SERIAL OUTPUT CLOCK LINE, A BI-DIRECTIONAL SERIAL DATA CLOCK LINE, AND OTHER MISC. CONTROL LINES DESCRIBED IN THE CHAPTER CALLED "SERIAL PORT PROTOCALL". DATA IS TRANSMITTED AND RECEIVED AS 8 BITS OF SERIAL DATA PRECEEDED BY A LOGIC ZERO START BIT, AND SUCCEEDED BY A LOGIC TRUE STOP BIT. INPUT AND OUTPUT CLOCKS ARE EQUAL TO THE BAUD (BIT) RATE, NOT 16 TIMES BAUD RATE. TRANSMITTED DATA CHANGES WHEN THE OUTPUT CLOCK GOES TRUE. RECEIVED DATA IS SAMPLED WHEN THE INPUT CLOCK GOES TO ZERO.

SERIAL OUTPUT THE TRANSMISSION SEQUENCE BEGINS WHEN THE PROCESSOR WRITES 8 BITS OF PARALLEL DATA INTO THE SERIAL OUTPUT REGISTER (SEROUT) (SEE AUDIO + SERIAL PORT BLOCK DIAGRAM). WHEN ANY PREVIOUS DATA BYTE TRANSMISSION IS FINISHED THE HARDWARE WILL AUTOMATICALLY TRANSFER NEW DATA FROM (SEROUT) TO THE OUTPUT SHIFT REGISTER, INTERUPT THE PROCESSOR TO INDICATE AN EMPTY (SEROUT) REGISTER (READY TO BE RELOADED WITH THE NEXT BYTE OF DATA), AND AUTOMATICALLY SERIALLY TRANSMITT THE SHIFT REGISTER CONTENTS WITH START-STOP BITS ATTACHED. IF THE PROCESSOR RESPONDS TO THE INTERUPT, AND RELOADS SEROUT BEFORE THE SHIFT REGISTER IS COMPLETLY TRANSMITTED, THE SERIAL TRANSMISSION WILL BE SMOOTH AND CONTINUOUS.

OUTPUT DATA IS NORMALLY TRANSMITTED AS LOGIC LEVELS (+4V = TRUE 0V = FALSE). DATA CAN ALSO BE TRANSMITTED AS TWO TONE INFORMATION. THIS MODE IS SELECTED BY BIT 3 OF SERCTL. IN THIS MODE AUDIO CHANNEL 1 IS TRANSMITTED IN PLACE OF LOGIC TRUE, AND AUDIO CHANNEL 2 IN PLACE OF LOGIC ZERO. CHANNEL 2 MUST BE THE LOWER TONE OF THE TONE PAIR.

THE PROCESSOR CAN FORCE THE DATA OUTPUT LINE TO ZERO (OR TO AUDIO CH. 2, IF IN TWO TONE MODE) BY SETTING BIT 7 OF SERCTL. THIS IS REQUIRED TO FORCE A BREAK (10 ZEROS) CODE TRANSMISSION.

SERIAL OUTPUT CLOCK

THE SERIAL OUTPUT DATA ALLWAYS CHANGES WHEN THE SERIAL OUTPUT CLOCK GOES TRUE. THE CLOCK THEN RETURNS TO ZERO IN THE CENTER OF THE OUTPUT DATA BIT TIME.

THE BAUD (BIT) RATE OF THE DATA AND CLOCK IS DETERMINED BY; AUDIO CHANNEL 4, AUDIO CHANNEL 2, OR BY THE INPUT CLOCK, DEPENDING ON THE SERIAL MODE SELECTED BY BITS 4,5,6 OF SERCTL. (SEE CHART AT END OF THIS SECTION)

SERIAL INPUT THE RECEIVING SEQUENCE BEGINS WHEN THE HARDWARE HAS RECEIVED A COMPLETE 8 BIT SERIAL DATA WORD PLUS START AND STOP BITS. THIS DATA IS AUTOMATICALLY TRANSFERED TO THE 8 BIT PARALLEL INPUT REGISTER (SERIN), AND THE PROCESSOR IS INTERUPTED TO INDICATE AN INPUT DATA BYTE READY TO BE READ IN SERIN. THE PROCESSOR MUST RESPOND TO THIS INTERUPT, AND READ SERIN, BEFORE THE NEXT INPUT DATA WORD RECEIPTION IS COMPLETE. OTHERWISE AN INPUT DATA "OVER-RUN" WILL OCCUR. THIS WILL BE INDICATED BY BIT 6 OF THE SERIAL PORT STATUS REGISTER (SKSTAT), AND MEANS INPUT DATA HAS BEEN LOST. THIS BIT SHOULD BE TESTED WHENEVER SERIN IS READ. BIT 7 OF SKSTAT SHOULD ALSO BE TESTED TO DETECT FRAME ERRORS CAUSED BY EXTRA (OR MISSING) DATA BITS.

DIRECT SERIAL INPUT THE SERIAL DATA INPUT LINE CAN BE READ DIRECTLY BY THE MICROPROCESSOR IF DESIRED, IGNORING THE SHIFT REGISTER, BY READING BIT 4 OF SKSTAT.

<u>BI-DIRECTIONAL CLOCK</u> THIS CLOCK LINE IS USED TO EITHER RECEIVE A CLOCK FROM AN EXTERNAL CLOCK SOURCE FOR CLOCKING TRANSMITTED OR RECEIVED DATA, OR IS USED TO SUPPLY A CLOCK TO EXTERNAL DEVICES INDICATING THE TRANSMIT OR RECEIPTION RATE. THIS CLOCK LINE DIRECTION IS DETERMINED BY THE SERIAL MODE SELECTED BY BITS 4,5,6 OF SERCTL. (SEE MODE CHART AT THE END OF THIS SECTION). TRANSMITTED DATA CHANGES ON THE RISING EDGE OF THIS CLOCK. RECEIVED DATA IS SAMPLED ON THE TRAILING EDGE OF THIS CLOCK.

<u>ASYNCHRONOUS SERIAL INPUT</u> UNCLOCKED SERIAL DATA (AT AN APPROXIMATELY KNOWN (±5%) RATE) CAN BE RECEIVED IN THE ASYNCHRONOUS MODES. THE RECEIVE (INPUT) SHIFT REGISTER IS CLOCKED BY AUDIO CHANNEL 4. CHANNELS 3 & 4 SHOULD BE USED TOGETHER (AUDCTL BIT 3=1) FOR INCREASED RESOLUTION. IN ASYNC. MODES, CHANNELS 3 AND 4 ARE RESET BY EACH START BIT AT THE BEGINNING OF EACH SERIAL DATA BYTE. THIS ALLOWS THE SERIAL DATA RATE TO BE SLIGHTLY DIFFERENT FROM THE RATE SET BY CHANNELS 3 & 4.

<u>SERIAL MODE CONTROL</u> THERE ARE 6 USEFULL MODES (OF THE POSSIBLE 8) CONTROLLED BY BITS 4,5,6 OF SERCTL. THESE ARE DESCRIBED ON THE NEXT PAGE.

NOTE THAT TWO TONE OUTPUT (BIT 3 OF SERCTL) MAY BE USED IN ANY OF THESE MODES EXCEPT FOR THE BOTTOM PAIR. THIS IS BECAUSE CHAN 2 IS USED TO SET THE OUTPUT TRANSMITT RATE AND IS THEREFORE NOT AVAILABLE FOR ONE OF THE 2 TONES.

NOTE THAT THE OUTPUT CLOCK RATE IS IDENTICAL TO THE OUTPUT DATA RATE.

SERIAL MODE CONTROL

(SEE ALSO REGISTER DESCRIPTION SERCTL)

FORCE BREAK

D7	D6	D5	D4	D3	D2	D1	D0

SERCTL REGISTER

POT SCAN AND KEYBOARD CTRL

TWO TONE CONTROL

MODE CONTROL BITS

(A) = ASYNCHRONOUS

D6	D5	D4	OUT RATE	= OUT CLOCK	IN RATE	BI-DIR CLOCK	COMMENTS
0	0	0	EXT.	EXT.	EXT.	EXT. INPUT	TRANS. + RECEIVE RATES SET BY EXTERNAL CLOCK ALSO INTERNAL CLOCK PHASE RESET TO ZERO
0	0	1	EXT.	EXT.	CHAN 4 (A)	EXT. INPUT	TRANS. RATE SET BY EXTERNAL CLOCK. RECEIVE ASYNCH. (CH 4)
0	1	0	CHAN. 4	CHAN. 4	CHAN. 4	CHAN. 4 OUTPUT	TRANS. + RECEIVE RATES SET BY CHAN. 4. CHAN. 4 OUTPUT ON BI-DIRECTIONAL CLOCK LINE
0	1	1	CH 4 (A)	CH 4 (A)	CH 4 (A)	INPUT	NOT USEFULL
1	0	0	CHAN. 4	CHAN. 4	EXT.	EXT. INPUT	TRANS. RATE SET BY CHAN 4. RECEIVE RATE SET BY EXTERNAL CLOCK
1	0	1	CH. 4 (A)	CH 4 (A)	CH 4 (A)	INPUT	NOT USEFULL
1	1	0	CHAN 2	CHAN 2	CHAN 4	CHAN 4 OUTPUT	TRANS. RATE SET BY CHAN 2 RECEIVE " " " " 4 CHAN 4 OUT ON BI-DIRECT. CLOCK LINE.
1	1	1	CHAN 2	CHAN 2	CHAN 4 (A)	INPUT NOT USED	TRANS. RATE SET BY CHAN 2. RECEIVE ASYNC. (CHAN 4) BI-DIR. CLOCK NOT USED

TWO TONE (BIT 3) NOT USEABLE IN THESE MODES

INTERUPT SYSTEM

GENERAL THERE ARE TWO BASIC TYPES OF INTERUPTS DEFINED ON THE MICROPROCESSOR; NMI (NON MASKABLE INTERUPT) AND IRQ (INTERUPT REQUEST) IT IS RECOMMENDED THAT A THOROUGH UNDERSTANDING OF THESE INTERUPT TYPES BE AQUIRED BY READING ALL CHAPTERS CONCERNING INTERUPTS IN THE 6502 MICROPROCESSOR PROGRAMING & HARDWARE MANUALS.

IN THIS SYSTEM NMI INTERUPTS ARE USED FOR VIDEO DISPLAY AND RESET. IRQ INTERUPTS ARE USED FOR SERIAL PORT COMMUNICATION, PERIPHERAL DEVICES, TIMERS, AND KEYBOARD INPUTS.

NMI INTERUPTS EVEN THOUGH NMI INTERUPTS ARE "UNMASKABLE" ON THE MICROPROCESSOR, THIS SYSTEM HAS INTERUPT ENABLE (MASK) BITS FOR EACH NMI FUNCTION. (BITS 5,6,7 OF NMIEN) WHEN THESE BITS ARE ZERO ALL NMI INTERUPTS ARE DISSABLED (MASKED) AND PREVENTED FROM CAUSING A MICROPROCESSOR NMI INTERUPT. (SEE NMIEN REGISTER DESCRIPTION) THE 3 TYPES OF NMI INTERUPTS ARE;

1. D7 = INSTRUCTION INTERUPT (DURING DISPLAY TIME ANY DISPLAY INSTRUCTION WITH BIT 7=1 WILL CAUSE THIS INTERUPT TO OCCUR (IF ENABLED) AT THE START OF THE LAST VIDEO LINE OF THE MODE)
2. D6 = VERTICAL BLANK INTERUPT (INTERUPT OCCURS (IF ENABLED) AT THE BEGINNING OF THE VERTICAL BLANK TIME INTERVAL.)
3. D5 = RESET BUTTON INTERUPT (PUSHING THE FRONT PANEL RESET BUTTON WILL CAUSE THIS INTERUPT TO OCCUR)

SINCE ANY OF THESE INTERUPTS WILL CAUSE THE PROCESSOR TO JUMP TO THE SAME NMI ADDRESS, THE SYSTEM ALSO HAS NMI STATUS BITS WHICH MAY BE EXAMINED BY THE PROCESSOR TO DETERMINE WHICH SOURCE CAUSED THE NMI INTERUPT. BITS 5,6,7 OF NMIST SERVE THIS FUNCTION. (SEE NMIST REGISTER DESCRIPTION) THESE STATUS BITS ARE SET BY THE CORRESPONDING INTERUPT FUNCTION (EVEN IF THE

INTERUPT IS MASKED FROM THE PROCESSOR BY NMIEN.) THE STATUS BITS MAY BE RESET TOGETHER BY WRITING TO THE ADDRESS NMIRES.

ALL THREE INTERUPT ENABLE BITS (BITS 5, 6, 7 OF NMIEN) ARE CLEARED AUTOMATICALLY DURING SYSTEM POWER TURN ON AND THEREFORE NMI INTERUPTS ARE INITALLY DISSABLED (MASKED), PREVENTING ANY POWER TURN ON SERVICE ROUTINE FROM BEING INTERUPTED BEFORE PROPER INITALIZATION OF REGISTERS AND POINTERS. THEY CAN THEN BE ENABLED BY THE PROCESSOR WHENEVER DESIRED, BY WRITING A 1 INTO BITS 5, 6, OR 7 OF NMIEN. EXCEPT FOR THE RESET BUTTON INTERUPT, THEY CAN ALSO BE DISSABLED BY THE PROCESSOR BY WRITING A ZERO INTO BITS 6 OR 7 OF NMIEN. ONCE ENABLED, THE RESET BUTTON CANNOT BE DISSABLED, ALLOWING AN UNSTOPABLE EXCAPE FROM ANY POSSIBLE "HANG UP" CONDITION.

THESE NMI INTERUPT FUNCTIONS ARE EACH SEPARATED IN TIME (TO PREVENT OVERLAPS) AND CONVERTED TO PULSES, BY THE SYSTEM HARDWARE, IN ORDER TO SUPPLY NMI TRANSISITIONS REQUIRED BY THE MICROPROCESSOR LOGIC.

IRQ INTERUPTS IRQ INTERUPTS ARE ALL "MASKABLE" TOGETHER BY ONE BIT OF THE STATUS REGISTER ON THE MICROPROCESSOR. THIS BIT IS SET TO THE DISSABLE CONDITION AUTOMATICALLY BY POWER TURN ON TO PREVENT INTERUPT OF POWER TURN ON SERVICE ROUTINES. IN ADDITION TO THIS PROCESSOR IRQ MASK BIT, THERE ARE SEPARATE SYSTEM IRQ INTERUPT ENABLE BITS FOR EACH IRQ INTERUPT FUNCTION (BITS 0 THRU 7 OF IRQEN). THESE BITS ARE NOT INITALIZED BY POWER TURN ON, AND MUST BE INITALIZED BY THE PROGAM BEFORE ENABELING THE PROCESSOR IRQ. THE 8 TYPES OF IRQ INTERUPTS ARE;

D7 = BREAK KEY (DEPRESSION OF THE BREAK KEY)
D6 = OTHER KEY (" OF ANY OTHER KEY)
D5 = SERIAL INPUT READY (BYTE OF SERIAL DATA HAS BEEN RECEIVED & IS READY TO BE READ BY THE PROCESSOR IN SERIN REGISTER)
D4 = SERIAL OUTPUT NEEDED (BYTE OF SERIAL DATA IS BEING TRANSMITTED AND SEROUT IS READY TO BE WRITTEN TO AGAIN BY THE PROCESSOR)
D3 = TRANSMISSION FINISHED (SERIAL DATA TRANSMISSION IS FINISHED. OUTPUT SHIFT REGISTER IS EMPTY)
D2 = TIMER #4 (AUDIO DIVIDER #4 HAS COUNTED DOWN TO ZERO)
D1 = TIMER #2 (AUDIO DIVIDER #2 HAS COUNTED DOWN TO ZERO)
D0 = TIMER #1 (AUDIO DIVIDER #1 HAS COUNTED DOWN TO ZERO

IN ADDITION TO THE ABOVE IRQ INTERUPTS (ENABLED BY BITS 0 THRU 7 OF IRQEN AND IDENTIFIED BY STATUS BITS 0 THRU 7 OF IRQST) THERE ARE TWO MORE SYSTEM IRQ INTERUPTS,

D7 OF PACTL = PERIPHERAL "A" INTERUPT STATUS BIT
D0 OF PACTL = PERIPHERAL "A" INTERUPT ENABLE BIT
D7 OF PBCTL = " "B" " STATUS BIT
D0 OF PBCTL = " "B" " ENABLE BIT

THESE LAST TWO INTERUPTS ARE AUTOMATICALLY DISABLED BY POWER TURN ON, AND THEIR STATUS BITS ARE RESET

BY READING FROM PORT A REGISTER AND PORT B REGISTER. (SEE PORTA, PACTL, PORTB, PBCTL REGISTER DESCRIPTIONS)

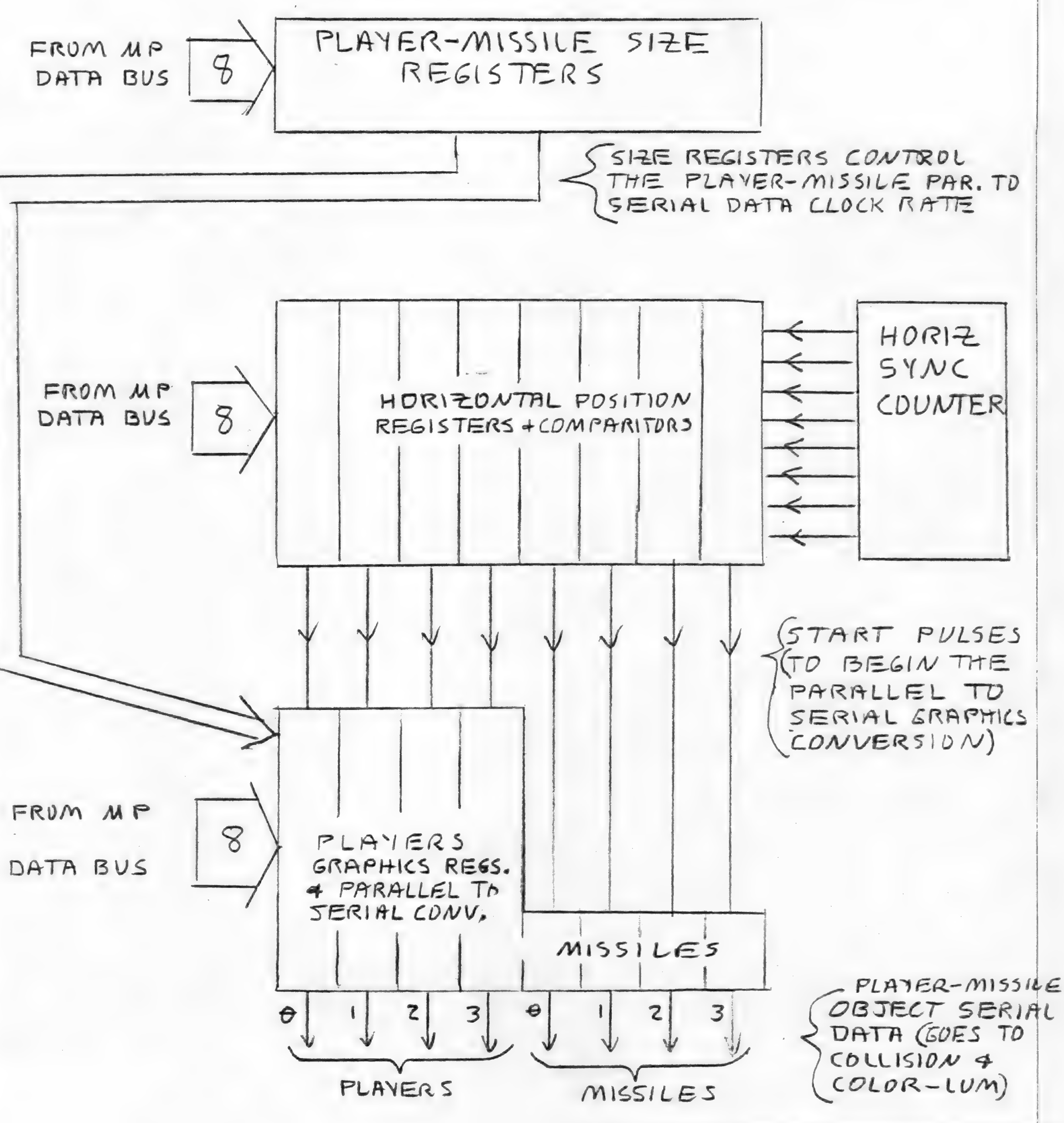
THE IRQEN REGISTER, LIKE THE NMIEN REGISTER, ENABLES INTERUPTS WHEN IT'S BITS ARE 1 (LOGIC TRUE). THE IRQST HOWEVER (UNLIKE THE NMIST) HAS INTERUPT STATUS BITS THAT ARE NORMALLY LOGIC TRUE, AND GO TO ZERO TO INDICATE AN INTERUPT REQUEST. THE IRQST STATUS BITS ARE RESET (RETURNED TO LOGIC TRUE) ONLY BY WRITING A ZERO INTO THE CORRESPONDING IRQEN BIT. THIS WILL DISABLE THE INTERUPT AND SIMULTANIOUSLY RESET (PUT TRUE) THE INTERUPT STATUS BIT.

* NOTE, BIT 3 OF IRQST IS NOT A LATCH AND DOES NOT GET RESET BY INTERUPT DISSABLE. IT IS TRUE WHEN THE SERIAL OUT IS EMPTY (OUT FINISHED) AND ZERO WHEN IT IS NOT.

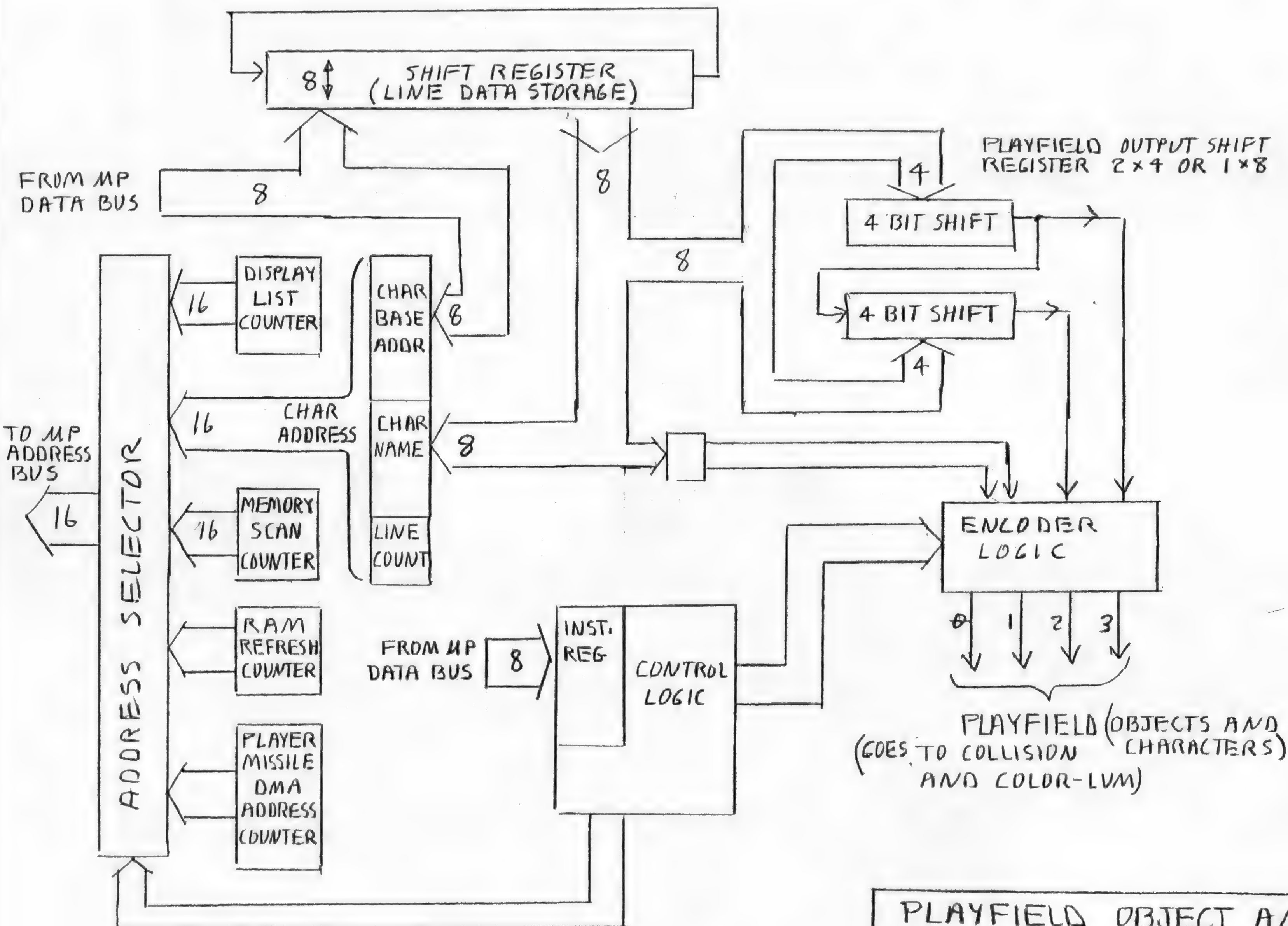
INTERUPT SUMMARY

NAME	FUNCTIONS	ENABLE	STATUS	← STATUS RESET
NMI INTERUPTS	DISPLAY INSTRUCT. VERT. BLK. RESET BUTTON	NMIEN (BITS 5, THRU 7) NORM. ZERO (DISSABLED)	NMIST (BITS 5, THRU 7) NORM. ZERO (NO INTERUPT)	ADDRESS NMIRES (RESETS ALL NMI STATUS TOGETHER)
IRQ INTERUPTS	KEYS SERIAL PORTS TIMERS	IRQEN (BITS 0, THRU 7) ZERO IS (DISSABLED) *	IRQST (BITS 0 THRU 7) NORM. TRUE (NO INTERUPT)	RESET (TO TRUE) BY ZERO IN CORRESPONDING BIT OF IRQEN (EXCEPT BIT 3) *
	PERIPH. A	D0 OF PACTL NORM. ZERO (DISSABLED)	D7 OF PACTL NORM. ZERO (NO INTERUPT)	RESET BY READING PORTA REGISTER
	PERIPH B	D0 OF PBCTL NORM ZERO (DISSABLED)	D7 OF PBCTL NORM. ZERO (NO INTERUPT)	RESET BY READING PORT B REGISTER

* NOTE. IRQEN IS NOT AUTOMATICALLY CLEARED AT POWER TURN ON.

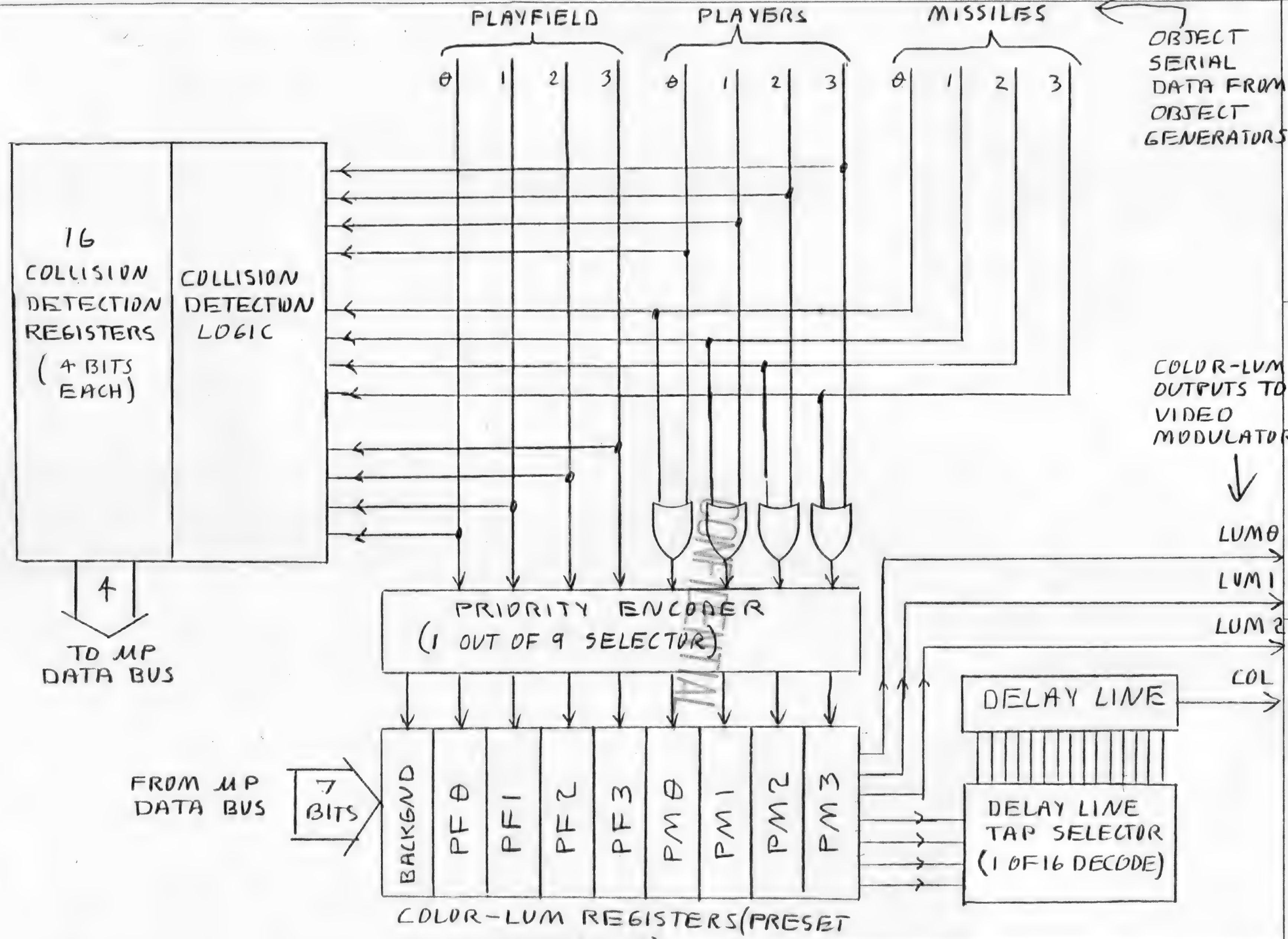


PLAYER-MISSILE OBJECT GENERATORS BLOCK DIAGRAM



PLAYFIELD OBJECT AND
CHARACTER GENERATOR
BLOCK DIAGRAM

BD2



COLLISION AND COLOR-LUM
BLOCK DIAGRAM

BD3

DMACTL (DIRECT MEMORY ACCESS CONTROL)

THIS ADDRESS WRITES DATA INTO THE DMA CONTROL REGISTER

NOT USED		D5	D4	D3	D2	D1	D0	
X	X	0	0	0	0	0	0	DMA DISPLAY INHIBIT *
						0	1	NARROW (128) — PLAYFIELD DMA ENABLE
						1	0	STANDARD (160) — PLAYFIELD DMA ENABLE
						1	1	WIDE (192) — PLAYFIELD DMA ENABLE
					1			MISSILE DMA ENABLE
				1				PLAYER DMA ENABLE
			1					PLAYER-MISSILE SINGLE LINE RESOLUTION
		1						INSTRUCTION FETCH DMA ENABLE

* NOTE; ALL ZERO IS POWER TURN ON CONDITION

DLISTL (DISPLAY LIST LOW)

THIS ADDRESS WRITES DATA INTO THE LOW BYTE OF THE DISPLAY LIST COUNTER.

D7	D6	D5	D4	D3	D2	D1	D0	
7	6	5	4	3	2	1	0	← DISPLAY LIST COUNTER BIT POSITION

DLISTH (DISPLAY LIST HIGH)

THIS ADDRESS WRITES DATA INTO THE HIGH BYTE OF THE DISPLAY LIST COUNTER

D7	D6	D5	D4	D3	D2	D1	D0	
15	14	13	12	11	10	9	8	← DISPLAY LIST COUNTER BIT POSITION

THE DISPLAY LIST IS A LIST OF DISPLAY INSTRUCTIONS IN MEMORY. THESE INSTRUCTIONS ARE ADDRESSED BY THE DISPLAY LIST COUNTER. LOADING THESE REGISTERS DEFINES THE ADDRESS OF THE BEGINNING OF THE DISPLAY LIST.

NOTE; THE TOP 6 BITS ARE LATCHES ONLY AND HAVE NO COUNT CAPABILITY, THEREFORE THE DISPLAY LIST CAN NOT CROSS A 1 K BYTE MEMORY BOUNDARY WITHOUT THE USE OF A JUMP INSTRUCTION

CHACTL (CHARACTER CONTROL)

THIS ADDRESS WRITES DATA INTO THE CHARACTER CONTROL REGISTER

NOT USED	D2	D1	D0

D2 CHARACTER VERTICAL REFLECT BIT
THIS BIT IS SAMPLED AT THE BEGINNING OF EACH LINE OF CHARACTERS. IF TRUE IT CAUSES THE LINE OF CHARACTERS TO REFLECT (INVERT) VERTICALLY.

D1. CHARACTER VIDEO INVERT FLAG (USED FOR 40 CHAR. MODE ONLY)
IF BIT 7 OF CHARACTER CODE IS TRUE THIS FLAG CAUSES THAT CHARACTER TO BE BLACK ON WHITE.

D0. CHARACTER BLANK (BLINK) FLAG (USED FOR 40 CHAR. MODE ONLY)
IF BIT 7 OF CHARACTER CODE IS TRUE THIS FLAG CAUSES THAT CHARACTER TO BLANK.

NMIEN (NON MASKABLE INTERUPT ENABLE)

THIS ADDRESS WRITES DATA TO THE NMI INTERUPT ENABLE BITS. WHEN THESE BITS ARE ZERO THE INTERUPTS ARE DISSABLED (MASKED).

D7	D6.	D5	NOT USED

D7. INSTRUCTION (DISP. LIST INST.) INTERUPT ENABLE
THIS BIT IS CLEARED BY POWER RESET, AND MAY BE SET OR CLEARED BY THE PROCESSOR.

D6. VERT. BLANK INTERUPT ENABLE
THIS BIT IS CLEARED BY POWER RESET, AND MAY BE SET OR CLEARED BY THE PROCESSOR

D5, RESET BUTTON INTERUPT ENABLE
THIS BIT IS CLEARED BY POWER RESET. IT MAY BE SET (BUT NOT CLEARED) BY THE PROCESSOR.

NMIST (NON MASKABLE INTERUPT STATUS)

THIS ADDRESS READS THE NMI STATUS REG.

D7	D6	D5	NOT USED

D7. THIS BIT IDENTIFIES AN NMI INTERUPT CAUSED BY BIT 7 OF A DISPLAY LIST INSTRUCTION

D6. THIS BIT IDENTIFIES AN NMI INTERUPT CAUSED BY THE BEGINNING OF VERTICAL BLANK

D5. THIS BIT IDENTIFIES AN NMI INTERUPT CAUSED BY THE RESET BUTTON.

NMIRES (NMI STATUS REG. RESET)

THIS WRITE ADDRESS RESETS THE NON MASKABLE INTERUPT STATUS REGISTER (NMIST).

NOT USED

CHBASE (CHARACTER ADDRESS BASE REGISTER)

THIS ADDRESS WRITES DATA INTO THE CHARACTER ADDRESS BASE REGISTER

D7	D6	D5	D4	D3	D2	D1	NOT USED

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE REG.							CHAR. NAME						CHAR. LINE		
CHARACTER ADDRESS															

PMBASE (PLAYER-MISSILE ADDRESS BASE REGISTER)

THIS ADDRESS WRITES DATA INTO THE PLAYER-MISSILE ADDRESS BASE REGISTER

D7	D6	D5	D4	D3	D2	NOT USED

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE REG.						PLAYER MISSILE SELECT			PLAYER-MISSILE SCAN COUNTER						
PLAYER-MISSILE ADDRESS															

HSCROLL (HORIZONTAL SCROLL REGISTER)

THIS ADDRESS WRITES DATA INTO THE HORIZONTAL SCROLL REGISTER

	D3	D2	D1	D0

0 TO 15 COLOR CLOCK RIGHT SHIFTS

NOTE; THIS NUMBER DEFINES THE NUMBER OF HORIZ. COLOR CLOCK RIGHT SHIFTS OF DISPLAYED DATA BEING HORIZONTALLY SCROLLED. DATA IS HORIZ. SCROLLED IF THE DISPLAY LIST INSTRUCTION CONTAINS A 1 IN IT'S H SCROLL FLAG BIT (BIT 4 OF INSTRUCTION BYTE)

VSCROL (VERTICAL SCROLL REGISTER)

THIS ADDRESS WRITES DATA INTO THE VERTICAL SCROLL REGISTER

	D3	D2	D1	D0

3 BITS USED FOR 8 LINE DISPLAY MODES

4 BITS USED FOR 16 LINE DISPLAY MODES

NOTE; THIS NUMBER DEFINES THE NUMBER OF UPWARD LINES OF VERTICAL PICTURE SHIFT IN ANY SCREEN AREA BEING VERTICALLY SCROLLED. DATA IS VERTICALLY SCROLLED IF THE DISPLAY LIST INSTRUCTION CONTAINS A 1 IN ITS VSCROLL FLAG BIT (BIT 5 OF INSTRUCTION BYTE). THE SCROLLED AREA WILL TERMINATE WITH THE FIRST INSTRUCTION HAVING A ZERO IN BIT 5.

VCOUNT (VERTICAL COUNTER)* SEE NOTE AT BOTTOM OF PAGE

THIS ADDRESS READS THE VERTICAL COUNTER (8 MOST SIGNIFICANT BITS)

D7	D6	D5	D4	D3	D2	D1	D0	
V8	V7	V6	V5	V4	V3	V2	V1	~~V0~~

V0 NOT READ. TWO LINE RESOLUTION SUPPLIED.

PENV (LIGHT PEN VERTICAL VALUE)

THIS ADDRESS READS THE VERTICAL LIGHT PEN REGISTER (8 MOST SIGNIFICANT BITS)

D7	D6	D5	D4	D3	D2	D1	D0	
LP8	7	6	5	4	3	2	1	~~0~~

LP0 NOT READ. TWO LINE RESOLUTION SUPPLIED

PENH (LIGHT PEN HORIZ. VALUE)

THIS ADDRESS READS THE HORIZONTAL LIGHT PEN REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
H7	H6	H5	H4	H3	H2	H1	H0

WSYNC (WAIT FOR HORZ. BLANK SYNCHRONISIM)

NOT USED

THIS ADDRESS SETS A LATCH THAT PULLS DOWN ON THE RDY LINE TO THE MICROPROCESSOR, CAUSING IT TO WAIT UNTILL THIS LATCH IS AUTOMATICALLY RESET BY THE BEGINNING OF HORIZONTAL BLANK,

*

VCOUNT	LINE #	
7C	0	VERTICAL BLANK
7D	2	
7E	4	
⋮	⋮	
03	21	
04	22	
05	24	
⋮	⋮	
7B	267	

GRACTL (GRAPHICS CONTROL)

THIS ADDRESS WRITES DATA TO THE GRAPHIC CONTROL REGISTER

NOT USED	D2	D1	D0

NOTE; DMACTL REGISTER ALSO CONTROLS PLAYER-MISSILE DMA

D2. ENABLE LATCHES ON TRIG 0 → TRIG 3 INPUTS (LATCHES ARE CLEARED AND TRIG 0 → TRIG 3 ACT AS NORMAL INPUTS WHEN THIS CONTROL BIT IS ZERO)

D1. ENABLE PLAYER DMA TO PLAYER GRAPHICS REGS.

D0. ENABLE MISSILE DMA TO MISSILE GRAPHICS REGS.

GRAFP0 → GRAFP3 (PLAYER GRAPHICS REGISTERS)

THESE ADDRESSES WRITE DATA DIRECTLY INTO THE PLAYER GRAPHICS REGISTERS, INDEPENDENT OF DMA.

D7	D6	D5	D4	D3	D2	D1	D0

LEFT — PLAYER ON TV SCREEN — RIGHT

GRAFM (MISSILE GRAPHICS REGISTER)

THIS ADDRESS WRITES DATA DIRECTLY INTO THE MISSILE GRAPHICS REGISTER, INDEPENDENT OF DMA.

D7	D6	D5	D4	D3	D2	D1	D0
L	R	L	R	L	R	L	R
M3		M2		M1		M0	

HPOSP0 → HPOSP3 (PLAYER HORIZ. POSITION)

THESE ADDRESSES WRITE DATA INTO THE PLAYER HORIZONTAL POSITION REGISTERS.

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	1	0	0	1	0	0	LEFT EDGE OF SCREEN
1	1	0	1	1	1	0	1	RIGHT EDGE OF SCREEN

HPOSM0 → HPOSM3 (MISSILE HORZ. POSITION)

THESE ADDRESS WRITES DATA INTO THE MISSILE HORIZONTAL POSITION REGISTERS

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	1	0	0	1	0	0	LEFT EDGE OF SCREEN
—	—	—	—	—	—	—	—	
1	1	0	1	1	1	0	1	RIGHT EDGE OF SCREEN

SIZEP0 → SIZEP3 (PLAYER SIZE)

THESE ADDRESSES WRITE DATA INTO THE PLAYER SIZE CONTROL REGISTERS

NOT USED	D1	D0	HORZ. SIZE REG. (PLAYER)
	0	0	NORMAL SIZE
	0	1	TWICE SIZE
	1	0	NORMAL SIZE
	1	1	4 TIMES SIZE

SIZEM (MISSILE SIZE)

THIS ADDRESS WRITES DATA INTO THE MISSILE SIZE CONTROL REGISTER.

D7	D6	D5	D4	D3	D2	D1	D0	HORZ. SIZE REG. (MISSILE)
M3		M2		M1		M0		
						0	0	NORMAL SIZE
						0	1	TWICE SIZE
						1	0	NORMAL SIZE
						1	1	4 TIMES SIZE

VDELAY (VERTICAL DELAY)

THIS ADDRESS WRITES DATA INTO THE VERTICAL DELAY REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
P3	P2	P1	P0	M3	M2	M1	M0

← WHEN OPERATING IN THE TWO LINE DMA MODE THESE BITS WILL MOVE THESE OBJECTS DOWN BY ONE TV LINE

COLPM0 → COLPM3 (PLAYER-MISSILE COLOR)

THESE ADDRESSES WRITE TO THE PLAYER-MISSILE COLOR-LUM REGISTERS. MISSILES HAVE THE SAME COLOR-LUM AS THEIR PLAYER UNLESS MISSILES ARE USED AS A 5 TH PLAYER (SEE BIT 4 OF "PRIOR")

D7	D6	D5	D4	D3	D2	D1	D0

(SEE "COLBAK" FOR BIT ASSIGNMENTS)

COLPF0 → COLPF3 (PLAYFIELD COLOR)

THESE ADDRESSES WRITE DATA TO THE PLAYFIELD COLOR-LUM REGISTERS.

D7	D6	D5	D4	D3	D2	D1	D0

(SEE COLBAK FOR BIT ASSIGNMENT)

COLBAK (BACKGROUND COLOR)

THIS ADDRESS WRITES DATA TO THE BACKGROUND COLOR-LUM REGISTER

D7	D6	D5	D4	D3	D2	D1	NOT USED	
X	X	X	X	0	0	0		ZERO LUMINANCE (BLACK)
				0	0	0		
				ETC				
				1	1	1		MAX LUMINANCE (WHITE)
0	0	0	0/1	GREY GOLD				
0	0	1	0/1					
0	1	0	0/1					
0	1	1	0/1					
1	0	0	0/1					
1	0	1	0/1					
0	1	0	0/1					
1	1	1	0/1					

PRIOR (PRIORITY)

THIS ADDRESS WRITES DATA INTO THE PRIORITY CONTROL REGISTER

	D5	D4	D3	D2	D1	DØ

D5. MULTI COLOR PLAYER ENABLE.

THIS BIT CAUSES THE LOGICAL "OR" FUNCTION OF THE BITS OF THE COLORS OF PLAYER Ø WITH PLAYER 1, AND ALSO OF PLAYER 2 WITH PLAYER 3. THIS PERMITS OVERLAPING THE POSITION OF 2 PLAYERS WITH A CHOICE OF 3 COLORS IN THE OVERLAPED REGION.

D4. FIFTH PLAYER ENABLE

THIS BIT CAUSES ALL MISSILES TO ASSUME THE COLOR OF PLAYFIELD TYPE 3. THIS ALLOWS MISSILES TO BE POSITIONED TOGETHER WITH A COMMON COLOR FOR USE AS A FIFTH PLAYER TYPE OBJECT.

D3, D2, D1, DØ. PRIORITY SELECT (MUTUALLY EXCLUSIVE)

THESE BITS SELECT ONE OF 4 TYPES OF PRIORITY. OBJECTS WITH HIGHER PRIORITY WILL APPEAR TO MOVE IN FRONT OF OBJECTS WITH LOWER PRIORITY.

HIGHER PRIORITY ↑

D3=1	D2=1	D1=1	DØ=1
PFØ	PFØ	PØ	PØ
PF1	PF1	P1	P1
PØ	PF2	PFØ	P2
P1	PF3 + P5	PF1	P3
P2	PØ	PF2	PFØ
P3	P1	PF3 + P5	PF1
PF2	P2	P2	PF2
PF3 + P5	P3	P3	PF3 + P5
BAK	BAK	BAK	BAK

TRIG0, TRIG1, TRIG2, TRIG3 (TRIGGER PORTS)

THESE ADDRESSES READ PORT PINS NORMALLY CONNECTED TO THE CONTROLLER TRIGGER BUTTONS.

NOT USED (ZERO FORCED)	D0

(ALL ARE READ IN D0)
(BUTTON ZEROS INPUT)
* SEE NOTE BELOW

CONSOL (CONSOLE SWITCH PORT)

THIS ADDRESS READS OR WRITES DATA FROM THE CONSOLE SWITCHES AND INDICATORS

NOT USED (ZERO FORCED)	D3	D2	D1	D0

ZEROS MUST BE WRITTEN TO THIS ADDRESS IN ORDER TO READ THE SWITCHES.
ONES WRITTEN WILL PULL DOWN ON THE SWITCH LINE.

* NOTE TRIG0 THRU TRIG3 ARE NORMALLY READ DIRECTLY BY μP (BIT 2 OF GRACTL = 0). IF BIT 2 OF GRACTL IS = 1 THESE INPUTS ARE LATCHED WHENEVER THEY GO TO LOGIC ZERO. THESE LATCHES ARE RESET (TRUE) WHEN BIT 2 OF GRACTL = 0.

M0PF, M1PF, M2PF, M3PF (MISSILE TO PLAYFIELD COLLISIONS)

THESE ADDRESSES READ MISSILE TO PLAYFIELD COLLISIONS.

NOT USED (ZERO FORCED)	D3	D2	D1	D0

3 2 1 0 ← PLAYFIELD TYPE

P0PF, P1PF, P2PF, P3PF (PLAYER TO PLAYFIELD COLLISIONS)

THESE ADDRESSES READ PLAYER TO PLAYFIELD COLLISIONS.

NOT USED (ZERO FORCED)	D3	D2	D1	D0

3 2 1 0 ← PLAYFIELD TYPE

M0PL, M1PL, M2PL, M3PL (MISSILE TO PLAYER COLLISIONS)

THESE ADDRESSES READ MISSILE TO PLAYER COLLISIONS

NOT USED (ZERO FORCED)	D3	D2	D1	D0

3 2 1 0 ← PLAYER TYPE

P0PL, P1PL, P2PL, P3PL. (PLAYER TO PLAYER COLLISIONS)

THESE ADDRESSES READ PLAYER TO PLAYER COLLISIONS

NOT USED (ZERO FORCED)	D3	D2	D1	D0

3 2 1 0 ← PLAYER TYPE

(PLAYER 0 AGAINST PLAYER 0 IS ALLWAYS A ZERO) ETC.

HITCLR (COLLISION "HIT" CLEAR)

THIS WRITE ADDRESS CLEARS ALL COLLISION BITS DESCRIBED ABOVE

NOT USED

POT0, → POT7 (POT VALUES)

THESE ADDRESSES READ THE VALUE (0 TO 228) OF 8 POTS CONNECTED TO THE 8 LINE POT PORT.

D8	D7	D6	D5	D4	D3	D2	D1	D0

EACH POT VALUE

THEY ARE VALID ONLY AFTER 228 TV LINES FOLLOWING THE "POTGO" COMMAND DESCRIBED BELOW

ALLPOT (ALL POT LINES SIMULTANIOUSLY)

THIS ADDRESS READS THE PRESENT STATE OF THE 8 LINE POT PORT.

D8	D7	D6	D5	D4	D3	D2	D1	D0

8 POT LINE STATES

CAPACITOR DUMP TRANSISTORS MUST BE TURNED OFF BY EITHER GOING TO FAST POT SCAN MODE (BIT 2 OF SERCTL) OR STARTING POT SCAN (POTGO)

POTGO (START POT SCAN)

NO DATA BITS USED

THIS WRITE ADDRESS STARTS THE POT SCAN SEQUENCE. THE POT VALUES (POT0 → POT7) SHOULD BE READ FIRST. THIS WRITE STROBE IS THEN USED CAUSING THE FOLLOWING SEQUENCE.

1. SCAN COUNTER CLEARED TO ZERO.
2. CAPACITOR DUMP TRANSISTORS TURNED OFF.
3. SCAN COUNTER BEGINS COUNTING
4. COUNTER VALUE CAPTURED IN EACH OF 8 REGISTERS (POT0 → POT7) AS EACH POT LINE CROSSES TRIGGER VOLTAGE.
5. COUNTER REACHES 228, CAPACITOR DUMP TRANSISTORS TURNED ON.

KBCODE (KEYBOARD CODE)

THIS ADDRESS READS THE KEYBOARD CODE, AND IS USEVALLY READ IN RESPONSE TO A KEYBOARD INTERUPT (IRQ AND BITS 6 OR 7 OF IRQST)

D7	D6	D5	D4	D3	D2	D1	D0

D7. = CNTL KEY
D6. = SHIFT KEY

ATTACH
KEY CODE HERE
LATER (ACTUAL + ASKI)

SKCTL (SERIAL PORT CONTROL

THIS ADDRESS WRITES DATA INTO THE REGISTER THAT CONTROLS THE CONFIGURATION OF THE SERIAL PORT, AND ALSO THE FAST POT SCAN AND KEYBOARD ENABLE.

D7	D6	D5	D4	D3	D2	D1	D0

(BITS ARE NORMALLY ZERO AND PERFORM THE FUNCTIONS SHOWN BELOW WHEN TRUE)

D7. FORCE BREAK (FORCE SERIAL OUTPUT TO ZERO(SPACE))

D6.
D5.
D4.
SERIAL PORT MODE CONTROL BITS (SEE MODE CHART AT END OF SERIAL PORT DESCRIPTION)

D3. TWO TONE (SERIAL OUTPUT TRANSMITTED AS TWO TONE SIGNAL INSTEAD OF LOGIC TRUE/FALSE.)

D2. FAST POT (FAST POT SCAN. THE POT SCAN COUNTER COMPLETES IT'S SEQUENCE IN TWO TV LINE TIMES INSTEAD OF ONE FRAME TIME. THE CAPACITOR DUMP TRANSISTORS ARE COMPLETLY DISSABLED)

D1. ENABLE KEY SCAN (ENABLES KEYBOARD SCANNING CIRCUIT)

D0. ENABLE DEBOUNCE (ENABLES KEYBOARD DEBOUNCE CIRCUITS)

$\overline{D0} \cdot \overline{D1}$ (BOTH ZERO) INITALIZE (ORIGINAL POWER ON STATE AND USED FOR TESTING)

SERIN (SERIAL INPUT DATA)

THIS ADDRESS READS THE 8 BIT PARALLEL HOLDING RECESTER THAT IS LOADED WHEN A FULL BYTE OF SERIAL INPUT DATA HAS BEEN RECEIVED. THIS ADDRESS IS USEUALLY READ IN RESPONSE TO A SERIAL DATA IN INTERUPT (IRQ AND BIT 5 OF IRQST)

D7	D6	D5	D4	D3	D2	D1	D0

SEROUT (SERIAL OUTPUT DATA)

THIS ADDRESS WRITES TO THE 8 BIT PARALLEL HOLDING REGISTER THAT IS TRANSFERED TO THE OUTPUT SERIAL SHIFT RECISTER WHEN A FULL BYTE OF SERIAL OUTPUT DATA HAS BEEN TRANSMITTED. THIS ADDRESS IS USUALLY WRITTEN IN RESPONSE TO A SERIAL DATA OUT INTERUPT (IRQ AND BIT 4 OF IRQST)

D7	D6	D5	D4	D3	D2	D1	D0

IRQST (IRQ INTERUPT STATUS)

THIS ADDRESS READS THE DATA FROM THE IRQ INTERUPT STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	DØ

THESE BITS ARE NORMALLY 1 (TRUE) AND GO TO ZERO TO INDICATE THE FOLLOWING FUNCTIONS

D7. =Ø= BREAK KEY INTERUPT
D6. =Ø= OTHER KEY INTERUPT
D5. =Ø= SERIAL INPUT DATA READY INTERUPT
D4. =Ø= SERIAL OUTPUT DATA NEEDED INTERUPT
D3 =Ø= SERIAL OUTPUT TRANSMISSION FINISHED INTERUPT *5
D2 =Ø= TIMER 4 INTERUPT
D1 =Ø= TIMER 2 INTERUPT
DØ =Ø= TIMER 1 INTERUPT

NOTE; SEE IRQ DESCRIPTION ON PG. 23 (NO DIRECT RESET ON BIT 3)

IRQEN (IRQ INTERUPT ENABLE)

THIS ADDRESS WRITES DATA TO THE IRQ INTERUPT ENABLE BITS. WHEN THESE BITS ARE ZERO THE INTERUPTS ARE DISSABLED (MASKED) AND THE CORRESPONDING BIT OF THE IRQST (IRQ INTERUPT STATUS REG) IS RESET (TO LOGIC TRUE)

D7	D6	D5	D4	D3	D2	D1	DØ

D7. BREAK KEY INTERUPT ENABLE
D6. OTHER KEY " "
D5. SERIAL INPUT DATA READY INTERUPT ENABLE
D4. " OUTPUT " NEEDED " "
D3. SERIAL OUT. TRANS. FINISHED INTERUPT ENABLE
D2. TIMER 4 " "
D1. TIMER 2 " "
DØ TIMER 1 " "

SKSTAT (SERIAL PORT-KEYBOARD STATUS)

THIS ADDRESS READS THE STATUS REGISTER GIVING INFORMATION ABOUT THE SERIAL PORT AND KEYBOARD.

D7	D6	D5	D4	D3	D2	D1	Dθ

(BITS ARE NORMALLY TRUE AND PROVIDE THE FOLLOWING INFORMATION WHEN ZERO)

D7. = θ = SERIAL DATA INPUT FRAME ERROR
D6. = θ = SERIAL DATA INPUT OVER-RUN
D5. = θ = KEYBOARD OVER-RUN
LATCHES MUST BE RESET = 1 (SKRES)

D4 = DIRECT FROM SERIAL INPUT PORT
D3 = θ = SHIFT KEY DEPRESSED
D2 = θ = LAST KEY IS STILL DEPRESSED
D1 = θ = SERIAL INPUT SHIFT REG. BUSY
Dθ NOT USED (LOGIC TRUE)

SKRES (RESET ABOVE STATUS REGISTER)

THIS WRITE ADDRESS RESETS BITS 7, 6, AND 5 OF THE SERIAL PORT-KEYBOARD STATUS REGISTER TO 1.

NO DATA BITS

RANDOM (RANDOM NUMBER GENERATOR)

THIS ADDRESS READS THE HIGH ORDER 8 BITS OF A 17 BIT POLYNOMIAL COUNTER (9 BIT, IF BIT 7 OF AUDCTL = 1)

D7	D6	D5	D4	D3	D2	D1	Dθ

STIMER (START TIMER)

THIS WRITE ADDRESS RESETS ALL AUDIO FREQUENCY DIVIDERS TO THEIR "AUDF" VALUE. THESE DIVIDERS GENERATE TIMER INTERUPTS WHEN THEY COUNT DOWN TO ZERO (IF ENABLED (IRQEN)).

NO DATA BITS

AUDCTL (AUDIO CONTROL)

THIS ADDRESS WRITES DATA INTO THE AUDIO MODE CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0

THESE DATA REGISTER BITS CONTROL AUDIO FUNCTIONS DESCRIBED BELOW

BIT 7 CHANGE 17 BIT POLY INTO A 9 BIT POLY

BIT 6 CLOCK CHAN. 1 WITH 1.79 MHZ, INSTEAD OF 64 KHZ

BIT 5 CLOCK CHAN 3 WITH 1.79 MHZ, INSTEAD OF 64 KHZ

BIT 4 CLOCK CHAN 2 WITH CHAN 1, INSTEAD OF 64 KHZ (16 BIT)

BIT 3 CLOCK CHAN 4 WITH CHAN 3, INSTEAD OF 64 KHZ (16 BIT)

BIT 2 INSERT HI PASS FILTER IN CHAN 1, CLOCKED BY CHAN 3.

BIT 1 INSERT HI PASS FILTER IN CHAN 2, CLOCKED BY CHAN 4.

BIT 0 CHANGE NORMAL 64 KHZ FREQ. INTO 15 KHZ

EXACT FREQUENCIES

THE FREQUENCIES GIVEN ABOVE ARE APPROXIMATE. THE EXACT FREQUENCY (FIN) THAT CLOCKS THE DIVIDE BY N COUNTERS IS GIVEN BELOW

FIN (APPROX)	FIN (EXACT)	
1.79 MHZ	1.78979 MHZ	— USE MODIFIED FORMULA FOR FOUT
64 KHZ	63.9210 KHZ	USE NORMAL FORMULA FOR FOUT
15 KHZ	15.6999 KHZ	USE NORMAL FORMULA FOR FOUT

THE NORMAL FORMULA FOR OUTPUT FREQUENCY IS,

$\boxed{F_{OUT} = F_{IN}/2N}$ WHERE N = THE BINARY NUMBER IN THE FREQ. REG (AUDF), PLUS 1. $(N = AUDF + 1)$

THE MODIFIED FORMULA SHOULD BE USED WHEN FIN = 1.79 MHZ AND A MORE EXACT RESULT IS DESIRED,

$$\boxed{F_{OUT} = \frac{F_{IN}}{2(AUDF + M)}}$$

WHERE; M = 4 IF 8 BIT COUNTER (AUDCTL BIT 3 OR 4 = 0)
M = 7 IF 16 BIT COUNTER (AUDCTL BIT 3 OR 4 = 1)

AUDF1, AUDF2, AUDF3, AUDF4 (AUDIO FREQUENCY)

THESE ADDRESSES WRITE DATA INTO EACH OF THE FOUR AUDIO FREQUENCY CONTROL REGISTERS. EACH REGISTER CONTROLS A DIVIDE BY "N" COUNTER

D7	D6	D5	D4	D3	D2	D1	D0	"N"
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
		ETC		↓				
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

NOTE; "N" IS ONE GREATER THAN THE BINARY NUMBER IN AUDIO FREQUENCY REGISTER AUDF(X)

AUDC1, AUDC2, AUDC3, AUDC4 (AUDIO CHANNEL CONTROL)

THESE ADDRESSES WRITE DATA INTO EACH OF THE FOUR AUDIO CONTROL REGISTERS.
EACH REGISTER CONTROLS THE NOISE CONTENT AND VOLUME OF THE CORRESPONDING AUDIO CHANNEL

DIVISOR "N" SET BY AUDIO FREQUENCY REGISTER

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0					17 BIT POLY ÷ 5 BIT POLY ÷ N
0	0	1	0					5 BIT POLY ÷ N ÷ 2
0	1	0	0					4 BIT POLY ÷ 5 BIT POLY ÷ N
0	1	1	0					5 BIT POLY ÷ N ÷ 2
1	0	0	0					17 BIT POLY ÷ N
1	X	1	0					PURE TONE ÷ N ÷ 2
1	1	0	0					4 BIT POLY ÷ N
X	X	X	1					FORCE OUTPUT (VOLUME ONLY)
			X	0	0	0	0	LOWEST VOLUME (OFF)
			X	1	0	0	0	HALF VOLUME
			X	1	1	1	1	HIGHEST VOLUME

PORTA (PORT A)

THIS ADDRESS READS OR WRITES DATA FROM PLAYER 0 AND PLAYER 1 CONTROLLER JACKS IF BIT 2 OF PACTL IS TRUE. THIS ADDRESS WRITES TO THE DIRECTION CONTROL REGISTER IF BIT 2 OF PACTL IS ZERO.

PORT A REGISTER (ADDRESSED IF BIT 2 OF PACTL IS TRUE)

D7	D6	D5	D4	D3	D2	D1	D0
R	L	B	F	R	L	B	F
JACK 1				JACK 0			

A DIRECTION CONTROL REGISTER (ADDRESSED IF BIT 2 OF PACTL IS ZERO)

D7	D6	D5	D4	D3	D2	D1	D0

DIRECTION OF JACK PINS
(0 = INPUT 1 = OUTPUT)

PACTL (PORT A CONTROL)

THIS ADDRESS WRITES OR READS DATA FROM THE PORT A CONTROL REGISTER.

PORT A CONTROL REG

D7	D6	D5	D4	D3	D2	D1	D0
READ ONLY	READ ONLY						
X	0	1	1	X	X	0	X

← SET UP REGISTER AS SHOWN
(X = DESCRIBED BELOW)

D2. CONTROLS PORTA ADDRESSING DESCRIBED ABOVE
(1 = PORT A REGISTER 0 = DIRECTION CONTROL REG.)

D3. PERIPHERAL MOTOR CONTROL
(0 = 1 =)

D7. (READ ONLY) PERPH. A INTERUPT STATUS BIT
(RESET BY READING PORT A REGISTER
SET BY PERIPHERAL A INTERUPT)

D0. PERIPHERAL A INTERUPT ENABLE BIT
(RESET BY POWER TURN ON OR PROCESSOR
SET BY PROCESSOR)

PORTB (PORT B)

THIS ADDRESS READS OR WRITES DATA FROM PLAYER 2 AND PLAYER 3 CONTROLLER JACKS IF BIT 2 OF PBCTL IS TRUE. THIS ADDRESS WRITES TO THE DIRECTION CONTROL REGISTER IF BIT 2 OF PBCTL IS ZERO

PORT B REGISTER (ADDRESSED IF BIT 2 OF PBCTL IS TRUE.)

D7	D6	D5	D4	D3	D2	D1	D0
R	L	B	F	R	L	B	F
JACK 3				JACK 2			

B DIRECTION CONTROL REGISTER (ADDRESSED IF BIT 2 OF PBCTL IS ZERO)

D7	D6	D5	D4	D3	D2	D1	D0

DIRECTION OF JACK PINS (0=INPUT 1=OUTPUT)

PBCTL (PORT B CONTROL)

THIS ADDRESS WRITES OR READS DATA FROM THE PORT B CONTROL REGISTER.

PORT B CONTROL REG

D7	D6	D5	D4	D3	D2	D1	D0
READ ONLY							
X	0	1	1	X	X	0	X

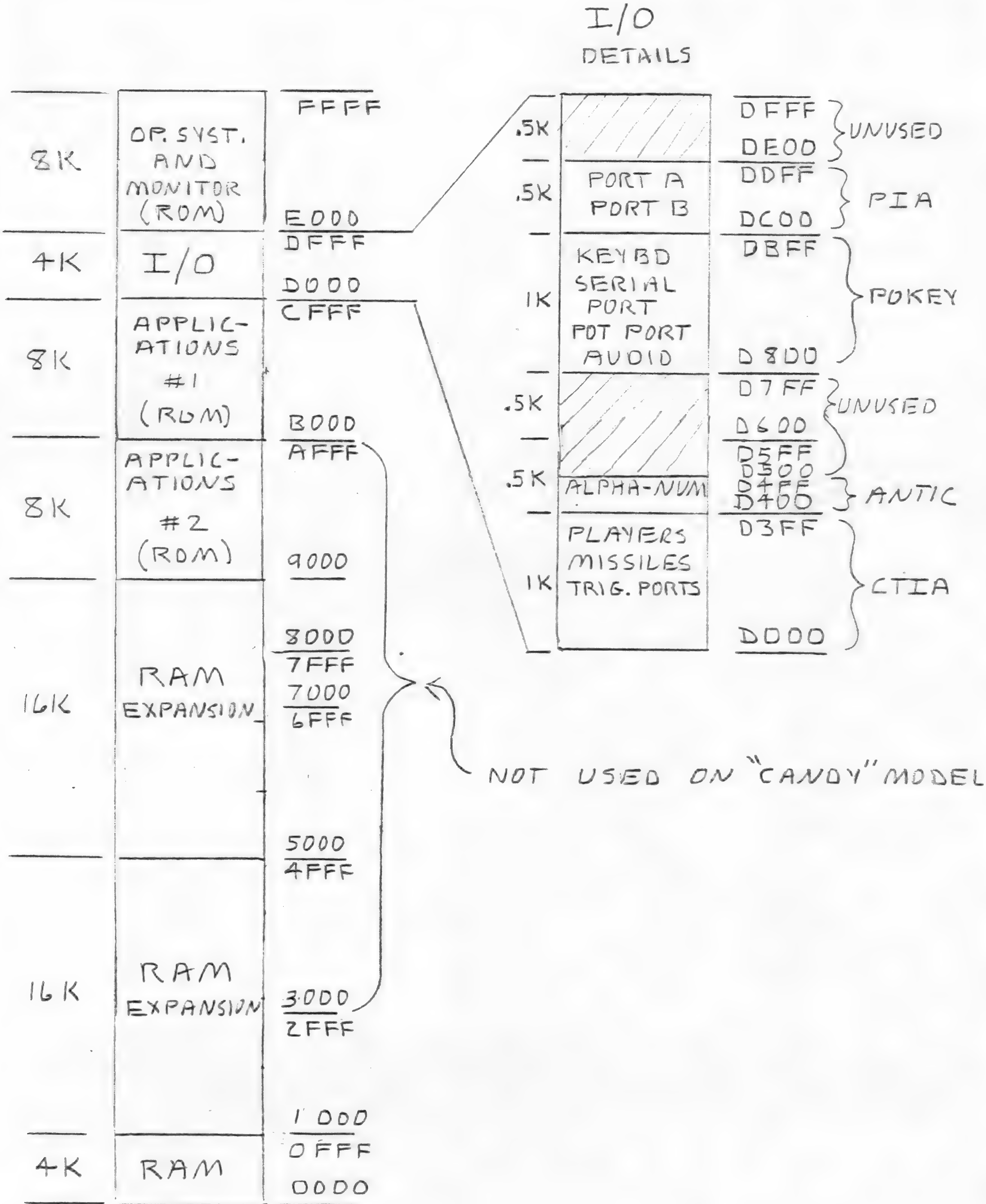
← SET UP REGISTER AS SHOWN (X=DESCRIBED BELOW)

D2. CONTROLS PORTB ADDRESSING DESCRIBED ABOVE (1 = PORT B REGISTER 0= DIRECTION CONTROL REG.)

D3. PERIPHERAL COMMAND IDENTIFICATION

D7. (READ ONLY) PERIPHERAL B INTERUPT STATUS BIT
(RESET BY READING PORT B REGISTER
SET BY PERIPHERAL B INTERUPT)

D0. PERIPHERAL B INTERUPT ENABLE BIT
(RESET BY POWER TURN ON OR PROCESSOR
SET BY PROCESSOR)


I/O DETAILS
8K
OP. SYST. AND MONITOR (ROM)
FFFF
E000
4K
I/O
DFFF
D000
8K
APPLIC-ATIONS #1 (ROM)
CFFF
B000
8K
APPLIC-ATIONS #2 (ROM)
AFFF
9000
16K
RAM EXPANSION
8000
7FFF
7000
6FFF
5000
16K
RAM EXPANSION
4FFF
3000
2FFF
4K
RAM
1000
0FFF
0000
NOT USED ON "CANDY" MODEL
.5K
DFFF
DE00
UNUSED
.5K
PORT A
PORT B
DDFF
DC00
PIA
1K
KEYBD
SERIAL PORT
POT PORT
AUDIO
DBFF
D800
POKEY
.5K
D7FF
D600
UNUSED
D5FF
D500
.5K
ALPHA-NUM
D4FF
D400
ANTIC
1K
PLAYERS
MISSILES
TRIG. PORTS
D3FF
D000
CTIA

MEMORY MAP

CTIA ADDRESSES

ADDRESS	WRITE NAME	WRITE DESCRIPTION	READ NAME	READ DESCRIPTION
D3FF ↕ D020	REPEAT AS BELOW 31 MORE TIMES			
D01F	CONSOL	WRITE CONSOL SW. PORT	CONSOL	READ CONSOL SW. PORT
D01E	HITCLR	COLLISION CLEAR		
D01D	GRACTL	GRAPHICS CONTROL		
D01C	VDELAY	VERT. DELAY		
D01B	PRIOR	PRIORITY SELECT		
D01A	COLBK	COL-LUM BKGND		
D019	COLPF3	COLOR-LUM OF PLAYFIELD 3		
D018	COLPF2	2		
D017	COLPF1	" 1		
D016	COLPFØ	" 0		
D015	COLPM3	COLOR-LUM OF PLAYER-MISSILE 3		
D014	COLPM2	2		
D013	COLPM1	" 1	TRIG3	READ CONTROLLER TRIGGER BUTTONS
D012	COLPMØ	" Ø	TRIG2	
D011	GRAFM	GRAPHICS ALL MISSILES	TRIG1	
D010	GRAFP3	GRAPHICS PLAYER 3	TRIG Ø	
D00F	GRAFP2	" " 2	P3 PL	READ PLAYER TO PLAYER COLLISIONS
D00E	GRAFP1	" " 1	P2 PL	
D00D	GRAFPØ	" " 0	P1 PL	
D00C	SIZEM	SIZE ALL MISSILES	PØ PL	
D00B	SIZEP3	SIZE PLAYER 3	M3 PL	READ MISSILE TO PLAYER COLLISIONS
D00A	SIZEP2	" " 2	M2 PL	
D009	SIZEP1	" " 1	M1 PL	
D008	SIZEPØ	" " Ø	MØ PL	
D007	HPOSM3	HORZ. POSIT. MISSILE 3	P3 PF	READ PLAYER TO PLAYFIELD COLLISIONS
D006	HPOSM2	" " " 2	P2 PF	
D005	HPOSM1	" " " 1	P1 PF	
D004	HPOSMØ	" " " Ø	PØ PF	
D003	HPOSP3	" " PLAYER 3	M3 PF	READ MISSILE TO PLAYFIELD COLLISIONS
D002	HPOSP2	" " " 2	M2 PF	
D001	HPOSP1	" " " 1	M1 PF	
D000	HPOSPØ	" " " Ø	MØ PF	

ANTIC ADDRESSES

ADDRESS	WRITE NAME	WRITE DESCRIPT.	READ NAME	READ DESCRIPT.
D4FF ↕ D410	} REPEAT	(AS BELOW)	15 MORE	TIMES
D40F	NMIRES	RESET NMI INTERUPT STATUS	NMIST	NMI INTERUPT STATUS REG.
D40E	NMIEN	NMI INTERUPT ENABLE		
D40D			PENV	LIGHT PEN REG. VERT
D40C			PENH	LIGHT PEN REG HORZ.
D40B			VCOUNT	VERTICAL LINE COUNTER
D40A	WSYNC	WAIT FOR HBLANK SYNCHRONISIM		
D409	CHBASE	CHARACTER BASE ADDRESS REG.		
D408				
D407	PMBASE	PLAYER-MISSILE BASE ADDRESS REG.		
D406				
D405	VSCROLL	VERT. SCROLL REG.		
D404	HSCROLL	HORIZ. SCROLL REG.		
D403	DLISTH	DISPLAY LIST POINTER (HIGH BYTE)		
D402	DLISTL	DISPLAY LIST POINTER (LOW BYTE)		
D401	CHACTL	CHARACTER CONTROL REG.		
D400	DMACTL	DMA CONTROL REG.		

POKEY ADDRESSES

	WRITE		READ	
	NAME	DESCRIPTION	NAME	DESCRIPTION
DBFF ↕ D810	REPEAT AS BELOW 63 MORE TIMES			
D80F	SKCTL	SERIAL PORT + KEY CONTROL	SKSTAT	SERIAL PORT + KEY STATUS REG.
D80E	IRQEN	IRQ INTERUPT ENABLE	IRQST	IRQ INTERUPT STATUS REG.
D80D	SEROUT	SERIAL PORT OUTPUT REG.	SERIN	SERIAL PORT INPUT REG.
D80C				
D80B	POTGO	START POT SCAN SEQUENCE		
D80A	SKRES	RESET STATUS (SKSTAT)	RANDOM	RANDOM NUMB. GENERATOR
D809	STIMER	START TIMERS	KBCODE	KEYBOARD CODE
D808	AUDCTL	AUDIO CONTROL	ALLPOT	READ 8 LINE POT PORT STATE
D807	AUDC4	AUDIO CHAN. 4 CONTROL	POT7	READ THE VALUE OF EACH POT
D806	AUDF4	AUDIO CHAN. 4 FREQUENCY	POT6	
D805	AUDC3	AUDIO CHAN. 3 CONTROL	POT5	
D804	AUDF3	AUDIO CHAN. 3 FREQUENCY	POT4	
D803	AUDC2	AUDIO CHAN. 2 CONTROL	POT3	
D802	AUDF2	AUDIO CHAN. 2 FREQUENCY	POT2	
D801	AUDC1	AUDIO CHAN. 1 CONTROL	POT1	
D800	AUDF1	AUDIO CHAN 1 FREQUENCY	POT0	

Change all D8xx to D2xx

PIA ADDRESSES

ADDRESS	WRITE NAME	WRITE DESCRIPTION	READ NAME	READ DESCRIPTION
D FF ↕ DC04	REPEAT AS SHOWN	BELOW MANY TIMES		
DC03	PBCTL	PORT B CONTROL	PBCTL	SAME AS WRITE
DC02	PACTL	PORT A CONTROL	PACTL	"
DC01	PORTB	DIRECTION REGISTER IF PBCTL BIT2 = 0 (OTHERWISE ↓)	PORTB	SAME AS WRITE
	PORT B	JACK 2 + JACK 3 IF DIRECTION BITS ARE 1 *	PORTB	JACK 2 + JACK 3 IF DIRECTION BITS ARE 0 *
DC00	PORTA	DIRECTION REGISTER IF PACTL BIT 2 = 0 (OTHERWISE ↓)	PORTA	SAME AS WRITE
	PORTA	JACK 0 + JACK 1 IF DIRECTION BITS ARE 1 *	PORTA	JACK 0 + JACK 1 IF DIRECTION BITS ARE 0 *

* NOTE; OUTPUT DATA IS RETAINED IN JACK OUTPUT REGISTERS. IF DIRECTION BITS ARE TRUE, A READ OF THE JACKS WILL READ OLD DATA FROM THESE REGISTERS.

POKEY PIN LIST (C012294)

NAME	TYPE	INTERNAL MAX. CAP.	DESCRIPTION
VDD			+5V POWER
VSS			GROUND
$\overline{CS0}$, CS1	IN	7PF	CHIP SELECTS
A0 - A3	IN	7 PF	ADDRESS BUS
Ø2	IN	14 PF	CLOCK FROM MP (1.78 MHZ)
R/W	IN	7 PF	READ-WRITE CONTROL
$\overline{IRQ}$	PD	15 PF	INTERUPT REQUEST TO MP
D0-D7	IN+TS	15 PF	DATA BUS
AUD	AU		AUDIO OUTPUT
$\overline{K0}$ - $\overline{K5}$	PD+R		KEYBOARD SCAN OUTPUTS
$\overline{KR1}$, $\overline{KR2}$	IN	7 PF	KEYBOARD SCAN INPUTS
P0 - P7	S+PD	15 PF	POT SCAN
SID	S	7 PF	SERIAL PORT INPUT DATA
SOD	PD	15 PF	SERIAL PORT OUTPUT DATA
BCLK	IN+PD	15 PF	BI-DIRECTIONAL SERIAL PORT CLOCK
OCLK	PD	15 PF	OUTPUT SERIAL PORT CLOCK

PIN #	NAME	PIN #	NAME
1	VSS	40	D2
2	D3	39	D1
3	D4	38	D0
4	D5	37	AUD
5	D6	36	A0
6	D7	35	A1
7	Ø2	34	A2
8	P7	33	A3
9	P6	32	R/W
10	P5	31	CS1
11	P4	30	$\overline{CS0}$
12	P3	29	$\overline{IRQ}$
13	P2	28	SOD
14	P1	27	OCLK
15	P0	26	BCLK
16	$\overline{KR2}$	25	$\overline{KR1}$
17	VDD	24	SID
18	$\overline{K5}$	23	$\overline{K0}$
19	$\overline{K4}$	22	$\overline{K1}$
20	$\overline{K3}$	21	$\overline{K2}$

CTIA PIN LIST (CO12295)

NAME	TYPE	INTERNAL MAX. CAP.	DESCRIPTION
VDD			+5 V POWER
VSS			GROUND
CSθ, $\overline{CS1}$	IN	7 PF	CHIP SELECTS
Aθ - A4	IN	7 PF	ADDRESS BUS
Ø2	IN	14 PF	CLOCK FROM μP (1.78 MHZ)
OSC	CLK	7 PF	OSCILLATOR INPUT (3.58 MHZ)
FØθ	PD+RD		FAST CLOCK TO ANTIC (3.58 MHZ)
R/W	IN	7 PF	READ-WRITE CONTROL
$\overline{HALT}$	IN	7 PF	HALT REQUEST FROM ANTIC
PAL	IN	14 PF	PAL COLOR CLOCK (PAL VERSION ONLY)
DEL	Y	50 PF	COLOR DELAY ADJUST
ANθ - AN2	IN	7 PF	VIDEO FROM ANTIC
CSYN	PD+RD		COMPOSITE SYNC OUTPUT
Lθ - L2	PD		LUMINANCE OUTPUT
COL	PD		COLOR OUTPUT
Dθ - D3	IN + TS	15 PF	DATA BUS
D4 - D7	IN + PD	15 PF	DATA BUS
Tθ - T3	IN + R	25 PF	TRIGGER INPUTS
Sθ - S3	IN + PD + R	25 PF	CONSOLE SWITCH INPUTS-OUTPUTS

PIN #	NAME	PIN #	NAME	PIN #	NAME
1	A1	40	A2		
2	Aθ	39	A3	16	DEL
3	VSS	38	A4	17	COL
4	D3	37	D4	18	PAL
5	D2	36	D5	19	ANθ
6	D1	35	D6	20	AN1
7	Dθ	34	D7	25	CSYN
8	Tθ	33	R/W	24	Lθ
9	T1	32	$\overline{CS1}$	23	L1
10	T2	31	CSθ	22	L2
11	T3	30	Ø2	21	AN2
12	Sθ	29	FØθ		
13	S1	28	OSC		
14	S2	27	VDD		
15	S3	26	$\overline{HALT}$		

STATIC PIN SPECS.

TYPE	PARAMETER	MIN	MAX	UNITS
IN (NORMAL INPUT)	INPUT LOGIC 0 LEVEL		0.8	VOLTS
	INPUT LOGIC 1 LEVEL	2.0		VOLTS
S (SCHMITT TRIGGER)	INPUT LOW THRESHOLD	1.0		VOLTS
	INPUT HIGH "	1.7	2.6	VOLTS
	HYSTERISIS	0.3		VOLTS
Y (COLOR ADJUST)	ADJUSTMENT RANGE	3.0	6.0	VOLTS
R (DEPLETION PU)	OUTPUT LOGIC 1 LEVEL @ -100 UA	2.4		VOLTS
RD (DRIVEN DEPLETION PULL UP)	OUTPUT LOGIC 1 LEVEL @ -200 UA	2.8		VOLTS
PD (PULL DOWN)	OUTPUT LOGIC 0 LEVEL @ 1.6 ma		0.4	VOLTS
PU (ENHANCEMENT PULL UP)	OUTPUT LOGIC 1 LEVEL @ -100 UA	2.4		VOLTS
PP (PUSH PULL)	SAME AS PD AND PU			
TS (TRI STATE)	SAME AS PD AND PU			
	PLUS OFF LEAKAGE @ 2.4 V		5	ua
AU (AUDIO OUT)	SEE NEXT PAGE			
CLK (CLOCK INPUT)	INPUT LOGIC 0 LEVEL		0.8	VOLTS
	INPUT LOGIC 1 LEVEL	2.4		VOLTS

CONFIDENTIAL

AUD (AUDIO OUTPUT)

Sixteen Open-Drain outputs in parallel (4 device sizes)

CHARACTERISTIC	MIN	TYP	MAX	UNIT
Measured with 10 KΩ pull-up to 4.7Vdc				
1 level	3.7		VCC	Vdc
Ø level (smallest device)			3.7	Vdc
Ø level (next)			2.9	Vdc
Ø level (next)			1.8	Vdc
Ø level (largest device)			1.2	Vdc

(Above are Stella Audio specs. presently tested for on Sentry).

Device "on" impedence @ 5v				
(small device)	14.3			KΩ
(next)	7.1			KΩ
(next)	3.6			KΩ
(largest device)	1.8			KΩ
Device "on" impedence @ 2.5v				
(small device)	8.8			KΩ
(next)	4.4			KΩ
(next)	2.2			KΩ
(largest device)	1.1			KΩ

ANTIC PIN LIST (C012296)

NAME	TYPE	INTERNAL MAX. CAP.	DESCRIPTION
VDD			+5V POWER
VSS			GROUND
Φ0	PD+RD	15 PF	CLOCK TO μP (1.78 MHZ)
Φ2	IN	15 PF	CLOCK FROM μP (1.78 MHZ)
R/W	IN+PU	7 PF	READ-WRITE CONTROL
$\overline{\text{HALT}}$	PP		HALT REQUEST TO μP AND CTIA
RDY	PP		WAIT REQUEST TO μP
$\overline{\text{NMI}}$	PP		INTERUPT REQUEST TO μP
FΦ0	CLK	7 PF	CLOCK FROM CTIA (3.58 MHZ)
$\overline{\text{RES}}$	IN		POWER ON RESET
$\overline{\text{LP}}$	S		LIGHT PEN INPUT
$\overline{\text{REF}}$	PP		REFRESH CONTROL TO RAMS
$\overline{\text{RNMI}}$	IN		RESET USING NMI INTERUPT
AN0-AN2	PP		VIDEO TO CTIA
A0-A3	IN+TS	15 PF	ADDRESS BUS
A4-A7	TS	15 PF	ADDRESS BUS
A8-A15	IN+TS	15 PF	ADDRESS BUS
D0-D7	IN+TS	15 PF	DATA BUS

PIN #	NAME	PIN #	NAME	PIN #	NAME
1	Vss	40	D7		
2	$\overline{\text{LP}}$	39	D6	16	A10
3	AN2	38	D5	17	A11
4	AN1	37	D4	18	A12
5	AN0	36	$\overline{\text{RES}}$	19	A13
6	$\overline{\text{RNMI}}$	35	FØ0	20	Ø2
7	$\overline{\text{NMI}}$	34	Ø0		
8	$\overline{\text{HALT}}$	33	D3	25	A8
9	$\overline{\text{REF}}$	32	D2	24	A9
10	A3	31	D1	23	A15
11	A2	30	D0	22	A14
12	A1	29	A4	21	VDD
13	A0	28	A5		
14	R/W	27	A6		
15	RDY	26	A7		

ATARI ANTIC CHIP, DISPLAY INSTRUCTI

COLORS: AB, APØ, AP1, AP2 — CODE 8 MEMORY MAP 32/40/48 CELLS (8/10/12 BYTES) 2 BITS

COLOR: AB, APØ — CODE 9 MEMORY MAP 64/80/96 CELLS (8/10/12 BYTES) 1 BIT

COLOR: AB, APØ, AP1, AP2 — CODE A MEMORY MAP 64/80/96 CELLS (16/20/24 BYTES) 2 BITS P

COLOR: AB, APØ 1 — CODE B, C MEMORY MAP 128/160/192 CELLS (16/20/24 BYTES) 1 BIT P

COLOR: AB, APØ, AP1, AP2 — CODE D, E MEMORY MAP 128/160/192 CELLS (32/40/48 BYTES) 2 BITS P

COLOR: AP2 LEV. AP2, AP1 — CODE F MEMORY MAP 256/320/384 CELLS (32/40/48 BYTES) 1 BIT PC

COLOR: AB, AP{CH7, CH6} — CODE 6, 7 5 COLOR 16/20/24 8×8 CELL CHARACTERS 1 BIT +2

BYTE

BYTES: 0 1 2 3 4 5 6 7

D7 D5 D3 D1 / D6 D4 D2 DØ — BIT ASSIGNMENTS

BYTE

BYTES: Ø 1 2 3 4 5 6 7

D7 D5 D3 D1 / D6 D4 D2 DØ — BIT ASSIGNMENTS

COLOR: AB, APØ, AP1, AP2 — CODE 4, 5 4 COLOR 32/40/48 4×8 CELL CHARACTERS 2 BITS P

BYTE

0 1 2 3 4 5 6 7

D7, D6 D3, D2 / D5, D4 D1, DØ — BITS

BYTES: 0 1 2 3 4 5 6 7

D7, D6 D3, D2 / D5, D4 D1, DØ — BITS

COLOR: AP2 LEV. AP1, AP2 — CODE 2 2 LEVEL 32/40/48 8×8 CELL CHARACTERS 1 BIT PE

BYTES: 0 1 2 3 4 5 6 7

D7 – DØ BITS

COLOR: AP2 LEV. AP1, AP2 — CODE 3 2 LEVEL 32/40/48 8×8 CELL CHARACTERS 1 BIT PE

BYTES: 0 1 2 3 4 5 6 7

2 3 4 5 6 7 0

D7 – DØ

CH6·CH5 – UPPER CASE

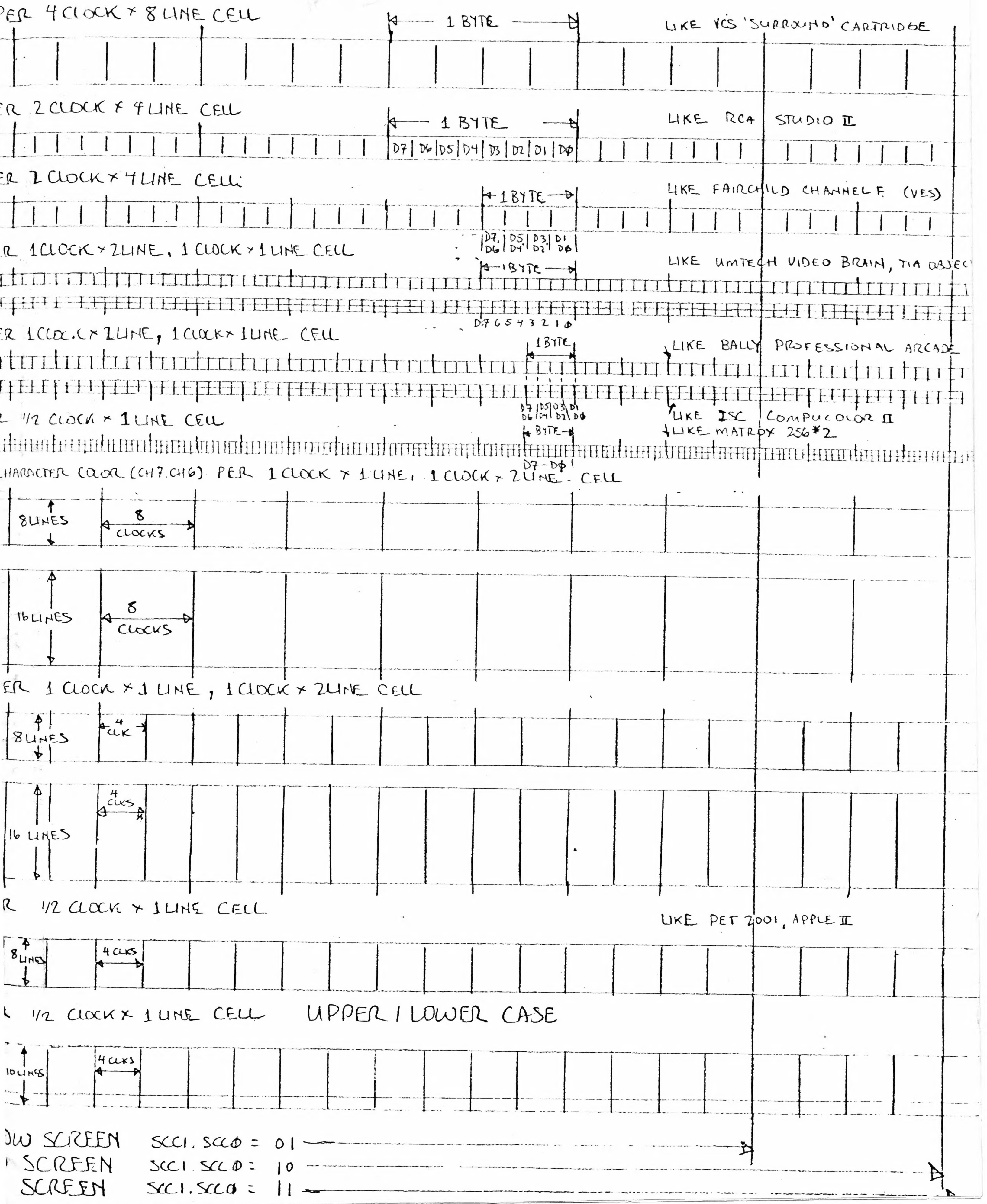
CH6·CH5 – LOWER CASE

128 COLOR CLOCKS — NARR

160 COLOR CLOCKS — STANDAR

192 COLOR CLOCKS — WIDE

ON FORMATS REV 1JUNE78 DECUIR



ATARI ANTIC

DECUIR

STATIC GRAPHICS GENERATION

PROGRAMMING MODEL   REV 1JUNE78

ANTIC AT D4ØØ

WRITE ADDRESS:

Addr									Name
Ø			DIE	PMR	PDE	MDE	SC1	SCØ	DMACTL DMA CONTROL
1						VREF	INV	BLANK	CHCTL CHARACTER CONTROL
2	DISPLAY LIST COUNTER LOW								DLISTL
3	DISPLAY LIST COUNTER HIGH								DLISTH
4					HORZ. SCROLL (CLOCKS)				HSCROLL
5					VERT. SCROLL (LINES)				VSCROLL
6 UNUSED									
7	PLAYER MISSLE BASE ADDRESS								PMBASE
8 UNUSED									
9	CHARACTER SET BASE ADDRESS								CH BASE
A	STROBE								WSYNC
C,D UNUSED									
(14) E	INMI	VNMI							NMIEN
(15) F	STROBE								NMIRES

READ ADDRESS:

Addr									Name
B	VERTICAL SYNC COUNTER (LINEPAIRS)								VCOUNT
C	LIGHT PEN HORIZONTAL (COLORCLOCKS)								PENH
D	LIGHT PEN VERTICAL (LINE PAIRS)								PENV
15 F	INST NMI	VBLK NMI	RES NMI						NMIST

DMA ADDRESSES:

"JUMP" ·I2	DLC7	DLC6	DLC5	DLC4	DLC3	DLC2	DLC1	DLCØ	L	DISPLAY LIST COUNTER/LATCH "DLC"
"JUMP" ·I3	DL15	DL14	DL13	DL12	DL11	DL10	DLC9	DL8	H	(SAME AS ABOVE)
JUMP· IR6·I2	MSC7	MSC6	MSC5	MSC4	MSC3	MSC2	MSC1	MSCØ	L	MEMORY SCAN COUNTER/LATCH
JUMP· IR6·I3	MSC15	MSC14	MSC13	MSC12	MSC11	MSC10	MSC9	MSC8	H	"MSC"
	BRI7	BRI6	BRI5	BRI4	BRI3	BRI2	BRI1	BRIØ		DISPLAY BUFFER RAM
	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SRØ		SERIAL DATA "ROUT" OUTPUT REGISTER
I_1	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IRØ		DISPLAY INSTRUCTION REGISTER "IR"
	NMI FLAG	← FLAGS →			← DISPLAY OP CODE →					SEE DESCRIPTION DETAILS IN TOP CENTER.

DMA CONTROL B

BITS Ø,1. PLAYFIELD

ØØ → NO DMA - B

WHOLE SCREEN

Ø1 → 'NARROW S

1Ø → 'STANDARD

11 → 'WIDE SC

BITS 4,3,2 PLAYER

BIT 2, MISSLE

BIT 3, PLAYER

BIT 4, Ø- LINE

BIT 5 - DISPLAY

CHARACTER CON

BIT Ø - BLANK C

BIT 1 - INVERT

BIT 2 - VERTICAL

INSTRUCTION

BIT Ø,1,2,3 - IN

BITS 4,5,6 - F

– BACKGROUND

BITS 6,5,4 =

– JUMP (COD

- BIT 6 - WI

BITS 5,4 UN

– DISPLAY IN

BIT 6 - LO

NEXT TWO

BITS - UF

Ø→1 BEC

1→Ø EN

BIT 4 - HC

BIT 7 NMI

LINE OF

ANTIC DMA ADDRESS FORMATS:

*

IT ASSIGNMENTS:

DMA

ACKROUND COLOR FOR
192 BK

REEN' 32BK-128-32BK

SCREEN' 16BK-160-16BK

REEN' 192 DISPLAY

MISSLES DMA

DMA ENABLE

MA ENABLE

PAIR RESOLUTION, 1 - SINGLE LINE

NSTRUCTION DMA ENABLE

TROL BIT ASSIGNMENTS:

HARACTER } '40/LINE TYPE
CHARACTER }

REFLECT

REGISTER BIT ASSIGNMENTS

STRUCTION OP CODE

AGS

(CODE ØØØØ)

UMBER OF LINES -1 (0-7) → (1-8)

E ØØØ1)

IT FOR VERTICAL SYNC

USED

STRUCTIONS (CODES 0010-1111)

AD MSC FLAG from

BYTES IN DISPLAYLIST

RTICAL SCROLL CONTROL

N VSCROLL

VSCROLL

RIZONTAL SCROLL ENABLE

ENABLE - ON LAST

CURRENT INSTRUCTION

	NAME	IR3-Ø CODE	DESCRIPTION (SEE DISPLAY MODE CHART FOR DETAIL)
Ø	"BLANK"	0000	1-8 LINES OF BACKGROUND COLOR
1	"JUMP"	0001	LOAD NEXT TWO BYTES INTO DISPLAY LIST COUNTER; DISPLAY 1 LINE BACKGROUND; IF IR6=1, HALT UNTIL NEXT FRAME
2	40/2 UC	0010	32/40/48 CHARACTERS/LINE 8×8×1 - EACH CELL ½ CLK×1 LINE - CH6 IS ADDRESS ONLY.
3	40/2 UR	0011	32/40/48 CHARACTERS/LINE 8×8×1 - SAME AS (0010) EXCEPT THAT CH6·CH5 = LOWER CASE - SHIFTS CHAR DOWN 2 LINES
4	40/4×1	0100	32/40/48 CHARACTERS/LINE 4×8×2 - EACH CELL 1 CLK×1 LINE 8 BYTES/CHAR - EACH BYTE 4 PAIRS ⇒ 3 COLORS + BACKGROUND @ EACH CELL
5	40/4×2	0101	32/40/48 CHARACTERS/LINE 4×8×2 - SAME AS (0100) EXCEPT THAT EACH CELL IS 1CLK×2LINES - WHOLE CHAR STRETCHED.
6	20/5×1	0110	16/20/24 CHARACTERS/LINE 8×8×1 EACH CELL 1CLK×1LINE CH7,CH6 DETERMINE COLOR FOR EACH BIT ON ⇒ 4 COLORS + BACKGROUND
7	20/5×2	0111	16/20/24 CHARACTERS/LINE 8×8×1 SAME AS (0110) EXCEPT THAT EACH CELL 1CLK×2 LINES
8	40×4	1000	32/40/48 MEMORY MAP CELLS EACH CELL 4CLK×8LINES EACH BYTE 4CELLS×2BITS → 3COLORS + BKGRN @ EACH CELL
9	80×2	1001	64/80/96 MEMORY MAP CELLS EACH CELL 2CLK×4LINES EACH BYTE 8CELLS×1BIT → 1COLOR + BKGRND @ EACH CELL
A	80×4	1010	64/80/96 MEMORY MAP CELLS EACH CELL 2CLK×4LINES EACH BYTE 4CELLS×2BITS → 3COLORS + BKGRND @ EACH CELL
B	160×2×2	1011	128/160/192 MEMORY MAP CELLS EACH CELL 1CLK×2LINES EACH BYTE 8CELLS×1BIT → 1COLOR + BKGRND @ EACH CELL
C	160×2×1	1100	128/160/192 MEMORY MAP CELLS EACH CELL 1CLK×1LINE EACH BYTE 8CELLS×1BIT → 1COLOR + BKGRND @ EACH CELL
D	160×4×2	1101	128/160/192 MEMORY MAP CELLS EACH CELL 1CLK×2LINES EACH BYTE 4CELLS×2BITS → 3COLORS + BKGRND @ EACH CELL
E	160×2×1	1110	128/160/192 MEMORY MAP CELLS - EACH CELL 1CLK×1LINE EACH BYTE 4CELLS×2BITS → 3COLORS + BKGRND @ EACH CELL
F	320×1	1111	256/320/384 MEMORY MAP CELLS - EACH CELL ½ CLK×1LINE EACH BYTE 8CELLS×1BIT - 2LEVELS @ BKGRND COLOR/CELL

ADDRESS/CHARACTER FORMATS BELOW

CHARACTER FORMATS:

"20/5" (0110,0111)

CHARACTER COLOR SELECT	- CHARACTER ADDRESS (8 BYTE CHAR) -

"40/2" (0010,0011)

INVERT/BLANK FLAG	CHARACTER ADDRESS (8 BYTE CHAR) -

CH6·CH5 → LOWER CASE

"40/4" (0100,0101)

TOGGLE COLOR	CHARACTER ADDRESS (8BYTE CHAR) -

→ TOGGLE COLOR - FORCE 10 CODE TO 11

	AB15	AB14	AB13	AB12	AB11	AB10	AB9	AB8	AB7	AB6	AB5	AB4	AB3	AB2	AB1	ABØ
RAM REFRESH	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	RF6	RF5	RF4	RF3	RF2	RF1	RFØ
TIA OBJECT SCAN RES: 2LINE	OB7	OB6	OB5	OB4	OB3	OB2	OS2	*OS1	OSØ	V7	V6	V5	V4	V3	V2	V1
TIA OBJECT SCAN RES: 1LINE	PM OB7	PM OB6	OB5	OB4	OB3	OS2	OS1*	OSØ	V7	V6	V5	V4	V3	V2	V1	VØ
DISPLAY LIST INSTR FETCH	DL15	DL14	DL13	DL12	DL11	DL10	DLC9	DLC8	DLC7	DLC6	DLC5	DLC4	DLC3	DLC2	DLC1	DLCØ
MEMORY SCAN (CHAR or MM)	MS15	MS14	MS13	MS12	MSC11	MSC10	MSC9	MSC8	MSC7	MSC6	MSC5	MSC4	MSC3	MSC2	MSC1	MSCØ
CHAR GRAPHICS FETCH '20/5'	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CH5	CH4	CH3	CH2	CH1	CHØ	ΔM2	ΔM1	ΔMØ
CHAR GRAPHICS FETCH 40/4 40/2	CB7	CB6	CB5	CB4	CB3	CB2	CH6	CH5	CH4	CH3	CH2	CH1	CHØ	ΔM2	ΔM1	ΔMØ

OS = OBJECT SELECT 011 = MISSLES 100 = PØ 110 = P2
101 = P1 111 = P3

ANTIC, SYSTEM RESOURCE CONSUMPTION

HOW MUCH RAM, HOW MUCH TIME	CHARACTER MAP OR MEMORY MAP IN BYTES, AND AS % OF 4096 (DISPLAY LIST AND CHAR SET NOT INCL)			NUMBER OF CYCLES USED FOR DISPLAY (INCL DL)/FRAME (AS % OF 262 LINES X (114 - 5 REFRESH) CYCLES/LINE).		
ACTIVE SCREEN SIZE	128 LINES × 128 CLOCKS	192 LINES × 160 CLOCKS	240 LINES × 192 CLOCKS	128 LINES × 128 CLOCKS	192 LINES × 160 CLOCKS	240 LINES × 192 CLOCKS
BACKGROUND, OR, DISPLAY INHIBITED	Φ	Φ	Φ	3	3	3
20/5 (2 LINE) CHARACTERS (512 BYTE CHARSET)	128 (3.12)	240 (5.9)	360 (8.8)	2202 (7.71)	4110 (14.39)	6153 (21.55)
20/5 (1 LINE) CHARACTERS (512 BYTE CHARSET)	256 (6.3)	480 (11.7)	720 (17.6)	2346 (8.21)	4374 (15.32)	6543 (22.91)
40/4 (2 LINE) CHARACTERS (1K BYTE CHARSET)	256 (6.3)	480 (11.7)	720 (35.2)	4394 (15.39)	8214 (28.76)	12303 (43.08)
40/4 (1 LINE) CHARACTERS (1K BYTE CHARSET)	512 (12.5)	960 (23.4)	1440 (35.2)	4650 (16.28)	8694 (30.44)	13023 (45.60)
40/2 (U CASE) CHARACTERS (1K BYTE CHARSET)	512 (12.5)	960 (23.4)	1440 (35.2)	4650 (16.28)	8694 (30.44)	13023 (45.60)
40/2 (U/L CASE) CHARACTERS (1K BYTE CHARSET)	416 (130 LINES) (10.2)	760 (190 LINES) (18.6)	1152 28.1	4599 (130 LINES) (16.10)	8379 (190 LINES) (29.34)	12696 (44.46)
40/4 COLOR (8 LINE × 4 CLOCK) MEM MAP	128 (3.1)	240 (5.9)	360 (8.8)	154 (0.54)	270 (0.95)	393 (1.38)
80/2 COLOR (4 LINE × 2 CLOCK) MEM MAP	256 (6.3)	480 11.7	720 (17.6)	298 (1.04%)	534 (1.87)	783 (2.74)
80/4 COLOR (4 LINE × 2 CLOCK) MEM MAP	512 (12.5)	960 (23.4)	1440 (35.2)	554 (1.94)	1014 (3.55)	1503 (5.26)
160/2 COLOR (2 LINE × 1 CLOCK) MEM MAP	1024 (25)	1920 (46.9)	2880 (70.3)	1098 (3.84)	2022 (7.08)	3003 (10.52)
160/2 COLOR (1 LINE × 1 CLOCK) MEM MAP	2048 (50)	3840 (93.8)	5760 (140.6)	2186 (7.65)	4038 (14.14)	6003 (21.02)
160/4 COLOR (2 LINE × 1 CLOCK) MEM MAP	2048 (50)	3840 (93.8)	5760 (140.6)	2122 (7.43)	3942 (13.80)	5883 (20.60)
160/4 COLOR (1 LINE × 1 CLOCK) MEM MAP	4096 (100)	7680 (187.5)	11520 (281.3)	4234 (14.86)	7878 (27.59)	11763 (41.19)
320/2 LEVEL (1 LINE × ½ CLK) MEM MAP	4096 (100)	7680 (187.5)	11520 (281.3)	4234 (14.86)	7878 (27.59)	11763 (41.19)
	CENTER OF SCREEN	STANDARD TV	MAXIMUM - ON MONITOR	CENTER OF SCREEN	STANDARD TV	MAXIMUM - ON MONITOR